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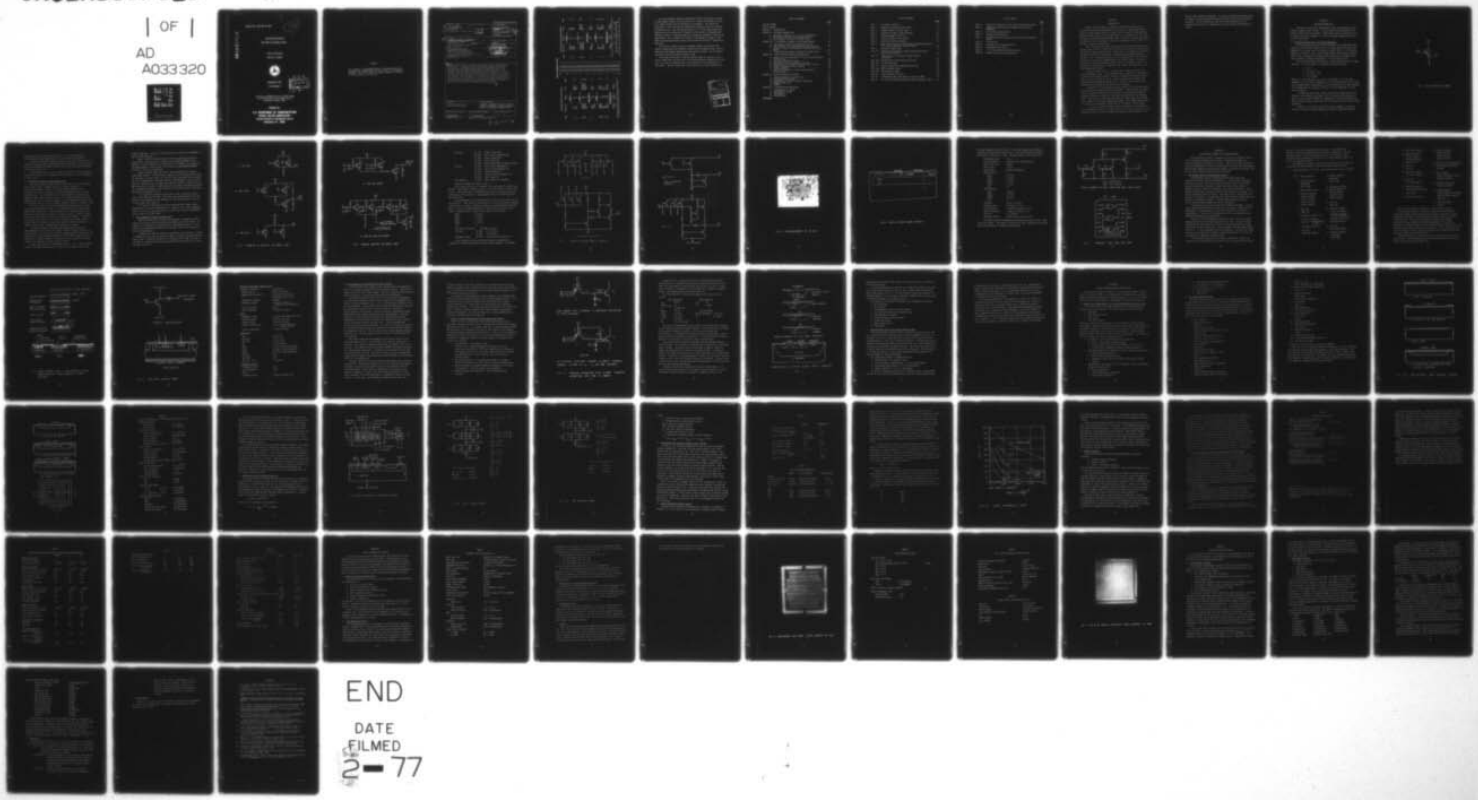

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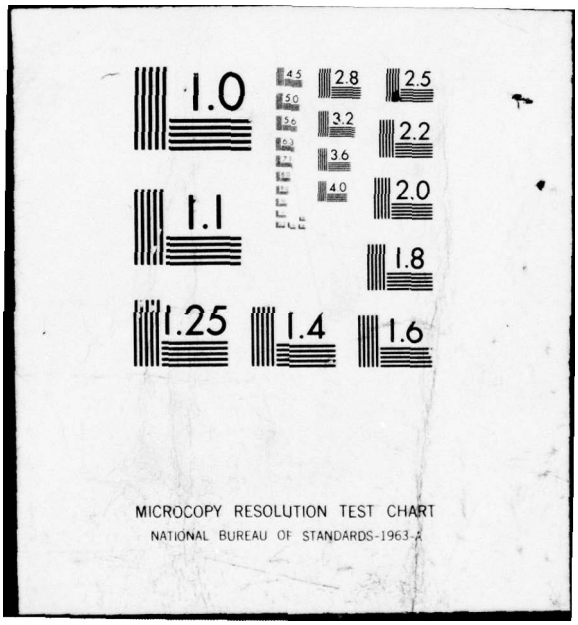
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AN EVALUATION OF EMITTER FOLLOWER LOGIC

Henry Domingos
Peter M. Capani

September 1976
Final Report

Prepared for

U.S. DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINISTRATION
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16. Abstract

Emitter follower logic is a non-saturating logic family with medium speed capabilities. When manufactured by a modernized planar non-epitaxial bipolar process, consistently high yields w th low defect densities are realized along with comparatively high device packing densities. The economical manufacturing technology coupled with the simplicity of emitter follower logic, provides a cost-effective means of approach to large scale and very large scale integrated circuit production. This report contains a description of th logic family, a h istory of the modernized planar process, descriptions and characteristics of emitter follower logic produced by this process and some examples of recently fabricated LSI and VLSI circuits. The report concludes with an evaluation of this technology.

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METRIC CONVERSION FACTORS

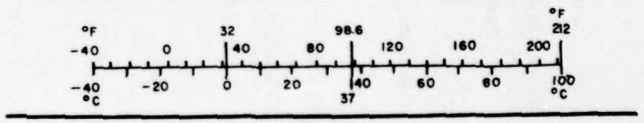
Approximate Conversions to Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
in	inches	*2.5	centimeters	cm
ft	feet	30	*centimeters*	cm
yd	yards	0.9	meters	m
mi	*miles*	1.6	kilometers	km
		AREA		
in^2	square inches	6.5	square centimeters	cm^2
ft^2	square feet	0.09	square meters	m^2
yd^2	*square yards*	*0.8*	*square meters*	m^2
mi^2	square miles	2.6	square kilometers	km^2
	acres	0.4	hectares	ha
		MASS (weight)		
oz	ounces	28	*grams*	g
lb	pounds	0.45	kilograms	kg
	short tons (2000 lb)	*0.9*	tonnes	t
		VOLUME		
tsp	teaspoons	5	milliliters	ml
Tbsp	tablespoons	15	milliliters	ml
fl oz	fluid ounces	30	milliliters	ml
c	cups	0.24	liters	l
pt	pints	0.47	liters	l
qt	quarts	0.95	liters	l
gal	gallons	3.8	liters	l
ft^3	cubic feet	0.03	cubic meters	m^3
yd^3	cubic yards	0.76	cubic meters	m^3
		TEMPERATURE (exact)		
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

*1 in = 2.54 (exactly). For other exact conversions and more detailed tables, see NBS Misc. Publ. 286, Units of Weights and Measures, Price $2.25, SD Catalog No. C13.10:286.

Approximate Conversions from Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
mm	*millimeters*	*0.04*	*inches*	*in*
cm	centimeters	0.4	inches	in
m	meters	3.3	*feet*	ft
m	meters	1.1	yards	yd
km	*kilometers*	0.6	miles	mi
		AREA		
cm^2	square centimeters	0.16	square inches	in^2
m^2	square meters	1.2	square yards	yd^2
km^2	square kilometers	0.4	square miles	mi^2
ha	hectares (10,000 m^2)	2.5	acres	
		MASS (weight)		
g	grams	0.035	ounces	oz
kg	*kilograms*	2.2	pounds	lb
t	tonnes (1000 kg)	1.1	short tons	
		VOLUME		
ml	*milliliters*	0.03	fluid ounces	fl oz
l	liters	2.1	pints	pt
l	liters	1.06	quarts	qt
l	liters	0.26	gallons	gal
m^3	cubic meters	35	cubic feet	ft^3
m^3	cubic meters	1.3	cubic yards	yd^3
		TEMPERATURE (exact)		
°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature	°F



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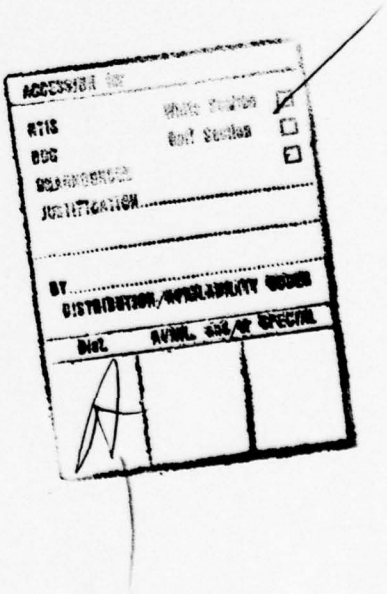

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SECTION I

INTRODUCTION

Emitter follower logic is a bipolar logic family which has been utilized in several custom-designed LSI circuits (1). When fabricated by a triple-diffused process, emitter follower logic is capable of high packing densities, high speeds, and very high yields. The implication is that this technology can produce high performance VLSI circuits at low cost and must be considered a serious contender to other LSI technologies such as LST^2L, I^2L, and MOS for future system design.

More than 50 circuits have been designed with triple diffused emitter follower logic (3D EFL). Fabricated circuits are used almost exclusively in Department of Defense applications. Design work is in progress for the Navy, Air Force, National Security Agency, and National Aeronautics and Space Administration. Systems which are or will be designed with 3D EFL circuits include IFF, secure voice communications, and various radars. LSI parts which have already been produced include a 64 bit correlator, a 16 x 16 bit multiplier, code generators, arithmetic logic arrays, FFT processors, and other random logic arrays.

Emitter follower logic is an older form of logic (2) which never achieved widespread use. It was sometimes used to replace the input diodes in certain logic families where, because the transistors provided current gain, it could increase the fan-in. No new logic design techniques were required since EFL behaved like DTL logic. However, other bipolar logic families were developed that proved to be more popular.

Fabrication by the 3D process closely duplicates the original planar process which was developed in the early 1960's. The technique was simpler than the standard bipolar process used today, but suffered from serious drawbacks relating to parasitic resistances and problems with saturating logic. Nevertheless, a few years ago emitter follower logic was combined with a planar, non-epitaxial fabrication scheme. With slight modification this came to be the present 3D EFL which is the subject of this report.

In order to assess the present logic technology it is necessary to become familiar with EFL as a logic family and to trace the evolution of its fabrication process from the original non-epitaxial planar method to the

present triple diffused technology. It is both interesting and instructive to observe the interrelationship between the logic family and the physical structure. In the following sections this interrelationship will be discussed fully because it determines the relative merits and drawbacks of 3D EFL.

SECTION II

EMITTER FOLLOWER LOGIC

The emitter follower has appeared from time to time during the past decade in digital logic circuits. In this section the properties of the emitter follower will be reviewed. Simple logic circuits utilizing it will be shown, and several examples of its use in standard commercial products will be illustrated.

A. The Emitter Follower as a Circuit Configuration

In the simplest sense, the emitter follower is an elementary bipolar transistor circuit whose collector is at a-c signal ground and whose load impedance is in series with its emitter as shown in Fig. 1. Its black-box behavior is similar to that of the cathode follower encountered in vacuum tube circuits, although it is apparent that vacuum tube and semiconductor devices cannot be compared operationally in the strictest sense.

The circuit functions primarily as a current amplifier with no signal inversion. Its small signal, low frequency properties include

1. $A_v < 1$
2. $A_I \approx h_{fe} + 1$
3. $Z_i \approx (h_{fe} + 1)R_L$
4. $Z_o < h_{ie}/h_{fe}$

where A_v is the voltage gain, A_I is the current gain, Z_i is the input impedance, Z_o is the output impedance, h_{fe} is the short-circuit current gain in the common emitter configuration, h_{ie} is the short-circuit input impedance in the common emitter connection, and R_L is the load impedance in series with the emitter.

Cascaded emitter follower stages attenuate the signal output level because of the cumulative V_{BE} drops. This is a distinct disadvantage of emitter follower logic and must be compensated for either by altering the input circuit operating conditions or by level restoring after several logic operations.

Because of its current gain and low output impedance the emitter follower is useful for output stages, line drivers, impedance matching

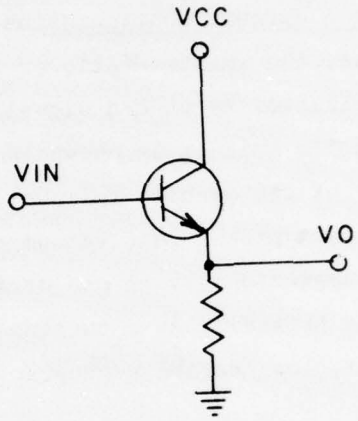


FIG. 1 THE EMITTER FOLLOWER

networks, and for driving capacitive loads. It is also suitable for interfacing with other logic families, such as diode logic circuits.

The emitter follower normally operates in the active region, with the operating point selected by adjusting the supply voltages. This means that the power dissipation per gate is high, and is one of the serious drawbacks to the use of EFL in LSI.

From another point of view, the emitter follower is nearly an ideal voltage switch with very low leakage in the off state and very low impedance in the on state.

B. The Emitter Follower in Logic Applications

The emitter follower lends certain characteristics to an integrated circuit logic family. Because there is no signal inversion, OR functions are obtained directly. Since the stages operate in a non-saturating mode they are capable of low gate propagation delays or high operating speed. The combination of low output impedance and high input impedance allows high fan-in and fan-out. For complex combinatorial logic implementation there is a certain amount of circuit design flexibility, and for integrated circuit layout the common collector region is a distinct asset.

Of course, there are certain disadvantages associated with a logic family based on emitter followers. As already mentioned, cascaded stages require level restoration. Power dissipation is a serious problem in LSI because the transistors are always in the active region. Emitter follower circuits are also inherently prone to parasitic oscillations. In addition, only logical OR functions can be directly realized with simple, single polarity emitter followers. Other logic functions require inverters (i.e., common emitter stages), complementary transistors, or diodes.

The disadvantages of fabricating both NPN and PNP transistors simultaneously on one chip are well known. Whether lateral, vertical, or composite PNP's are used, there are design compromises which can lead to low current gain and poor frequency response. Vertical PNP's require that the substrate be a common terminal for collectors. This restricts the design somewhat, but presents no serious problem for EFL.

Simple logic gates are illustrated in Fig. 2. Part A shows a simple OR gate. By adding an inverter as in part B of the figure, the OR gate

becomes a NOR gate. In Fig. 2C, PNP transistors are utilized to implement a simple positive AND gate.

Figure 3 shows a simple realization of more complicated functions using diodes. The A part of the figure shows the AND-OR-INVERT (A-O-I) function. The load impedance for transistor T3 is assumed to be provided by succeeding stages. In the B part of the figure the AND-OR-AND-OR-INVERT (A-O-A-O-I) function is implemented.

Emitter follower logic has several subtle advantages for complex random logic design. If several power supplies can be tolerated and if there are inverters in a logic chain, the need for level restoration can be avoided. The use of complementary transistors presents an advantage in circuit layout since the collectors are all common and connected to ground. With the use of PNP transistors all forms of simple gates are available, eliminating the need for intermediate inversions. The end result is that EFL can be an efficient, high density technology for LSI.

It is possible to fabricate current mode logic or emitter coupled logic on the same chip with EFL. This means that different parts of an LSI circuit can be designed to take advantage of the unique features of any one of these three logic families.

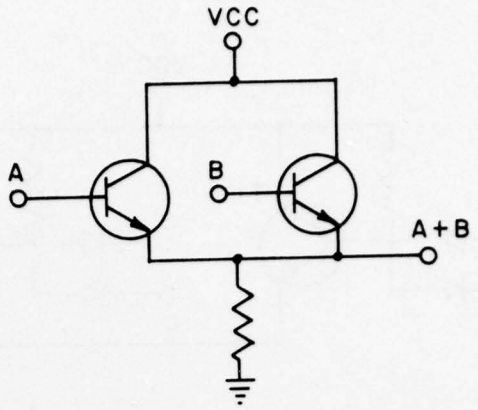
T^2L cannot be fabricated on the same chip with EFL without certain modifications, as will be explained later. However, EFL is fully compatible with T^2L in that the required interface circuits can be easily incorporated into the rest of the EFL design.

C. Early Examples of Emitter Follower Logic

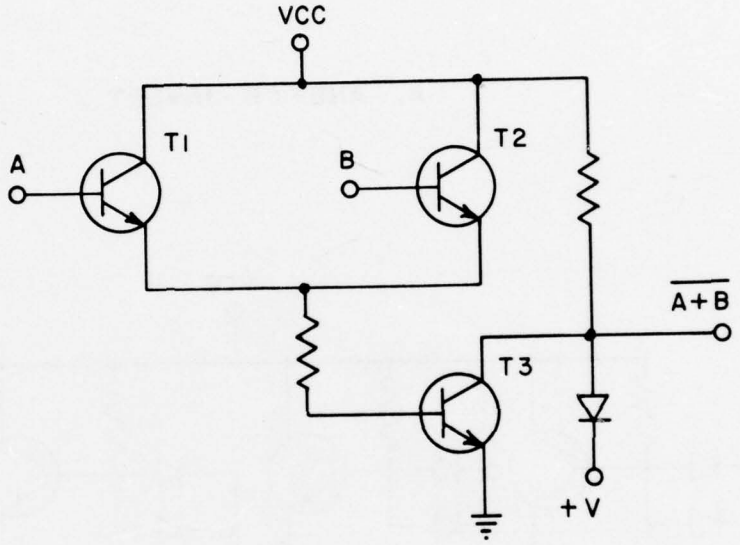
Emitter follower logic circuits have appeared in commercial product lines of at least two major semiconductor manufacturers in the 1960's. One example is the Signetics Corporation family trade-named Utilogic II. The other is the Complementary Transistor Micro-Logic family (CTμL) offered by Fairchild Semiconductor.

Although the Signetics Corporation advertises their Utilogic II family of integrated circuits as TTL and DTL, examples of emitter follower logic are easily found. Originally offered as the Utilogic line in 1964, Utilogic II provides the following circuits which use emitter follower logic in at least one logic level (3):

A. OR GATE



B. NOR GATE



C. AND GATE

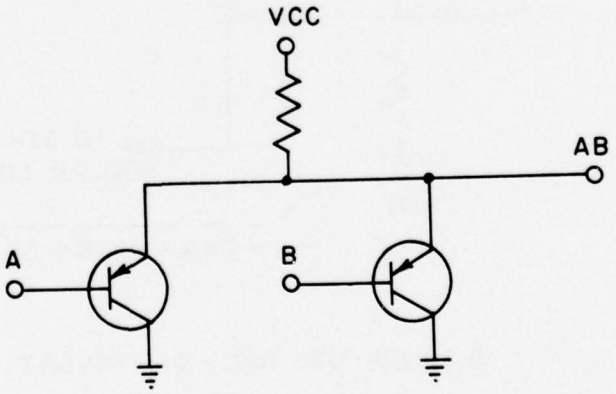
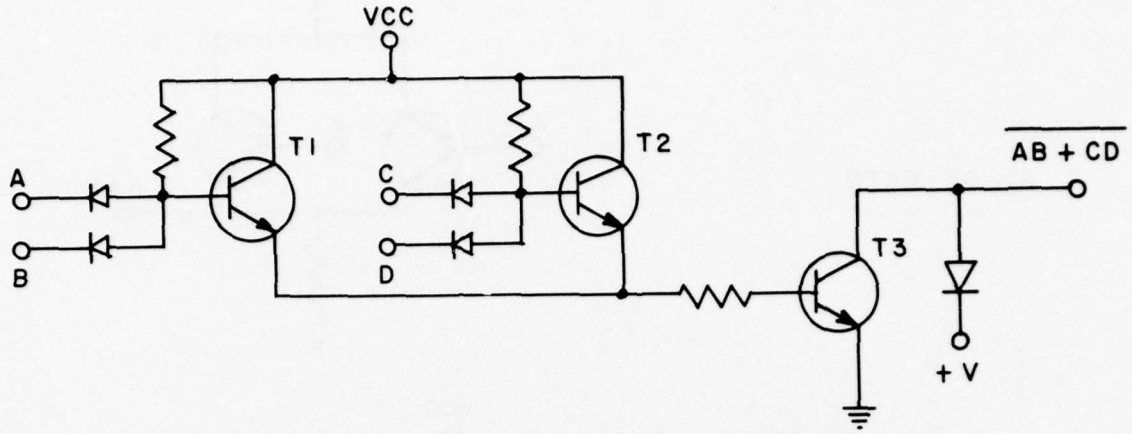
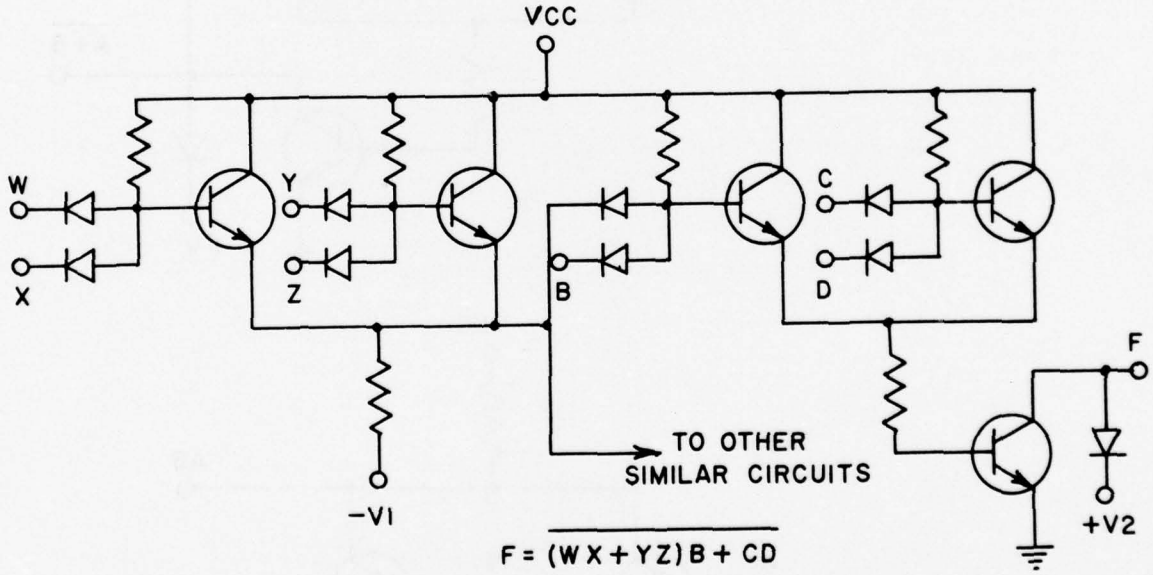


FIG. 2 EXAMPLES OF EMITTER FOLLOWER LOGIC



A. AND - OR - INVERT



B. AND - OR - AND - OR - INVERT

FIG. 3 COMPLEX EMITTER FOLLOWER LOGIC

NOR Gates	SP 314A	Single 7-input NOR
	SP 317A	Dual 4-input expandable NOR
	SP 370A	Triple 3-input NOR
	SP 380A	Quad 2-input NOR
	SP 381A	Quad 2-input NOR with open collector
OR Gates	SP 333A	Dual 3-input expandable OR
	SP 334A	Dual 4-input expandable OR
	SP 374A	Triple 3-input OR
	SP 375A	Triple 2-input expandable OR
	SP 384A	Quad 2-input OR
Gate Expanders	SP 300A	Dual 3-input gate expander

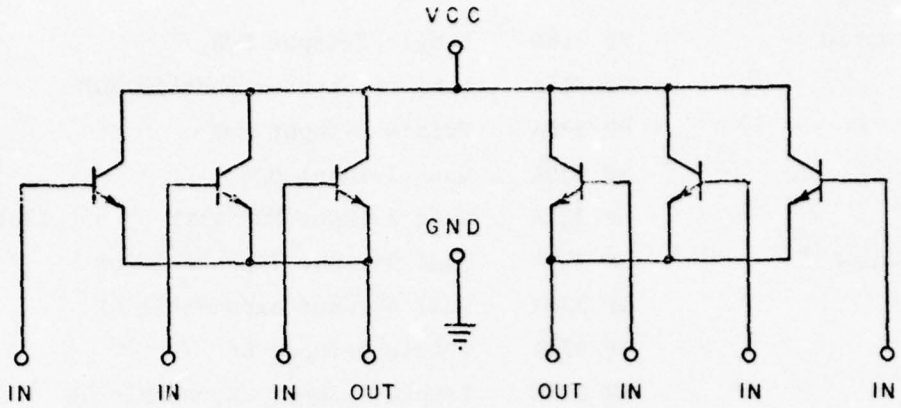
Schematic diagrams are shown in Fig. 4.

All of these circuits are available in a 14-pin plastic dual-in-line package. Power supply voltage is 5 volts. The noise margin is greater than 1 volt. The OR gates have a propagation delay of 45 ns typical and a gate dissipation of 55 mW typical. Corresponding values for the NOR gates are 40 ns and 30 mW.

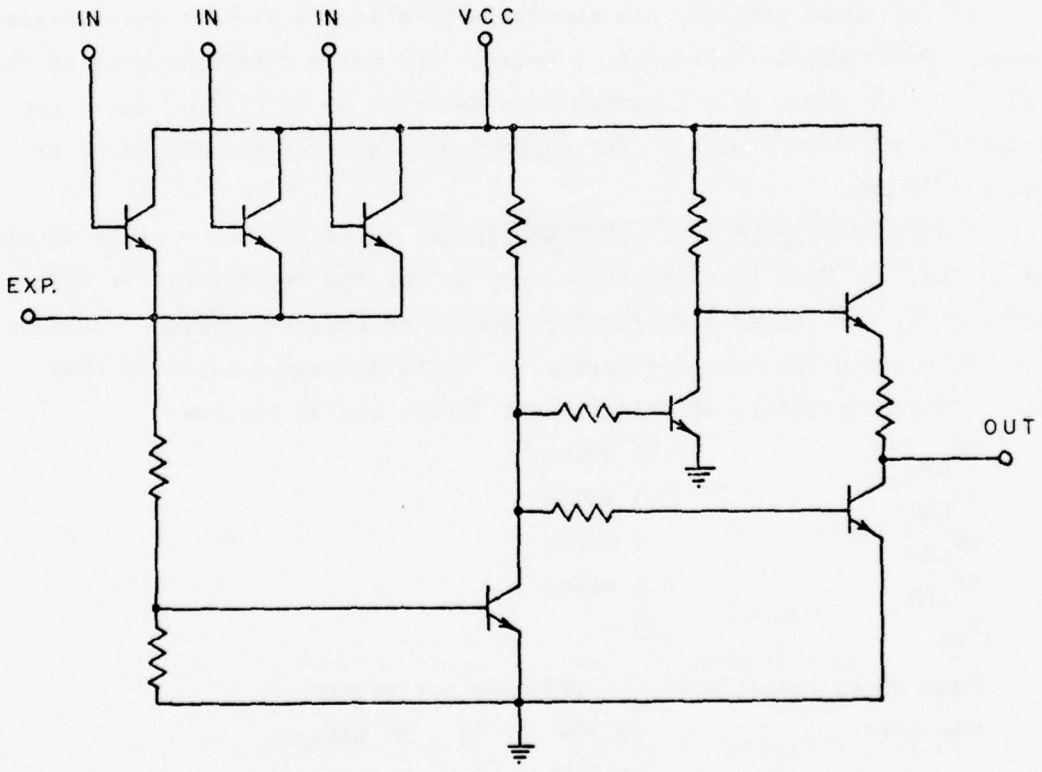
A photomicrograph of the SP374A appears in Fig. 5 and a cross section view in Fig. 6. Note that the technology is not the typical planar epitaxial construction, but rather a diffused collector or triple-diffused technique. Hence, it bears a striking similarity to 3D EFL discussed later in this report. Characteristics of this circuit family are as follows:

BV_{CSO}	42 volts	
BV_{CBO}	24 volts	
BV_{CEO}	7 volts	
BV_{EBO}	6.4 volts	
h_{FE}	25	
Base sheet resistivity	120 ohms per square	
Die size	SP 300	34 x 54 mils
	SP 374A	37 x 51 mils
Component density	SP 374A	15,000 parts per square inch

A good example of emitter follower logic with complementary transistors is the Fairchild CTμL-953 dual 4-input AND gate. A schematic

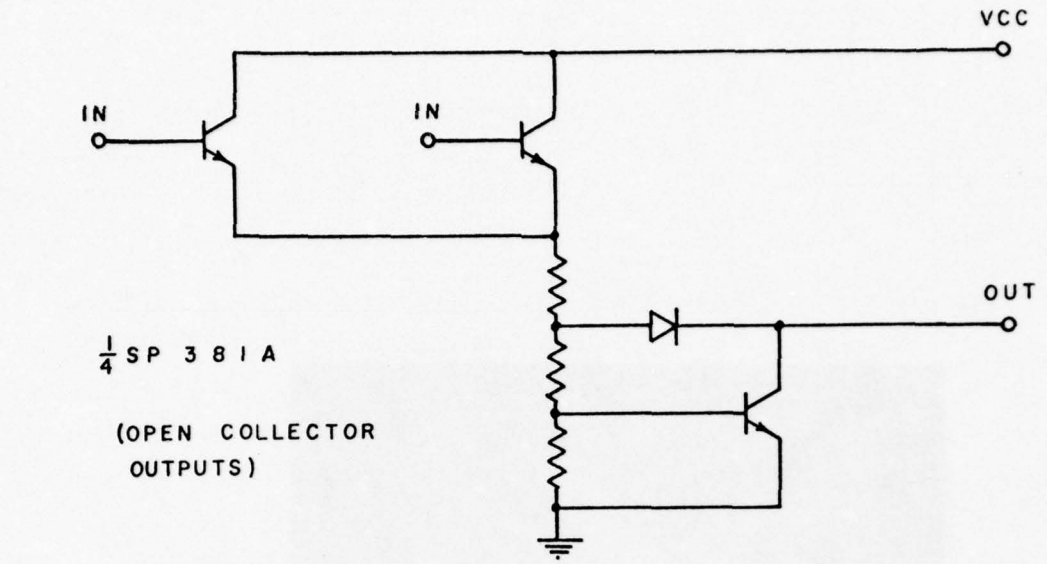


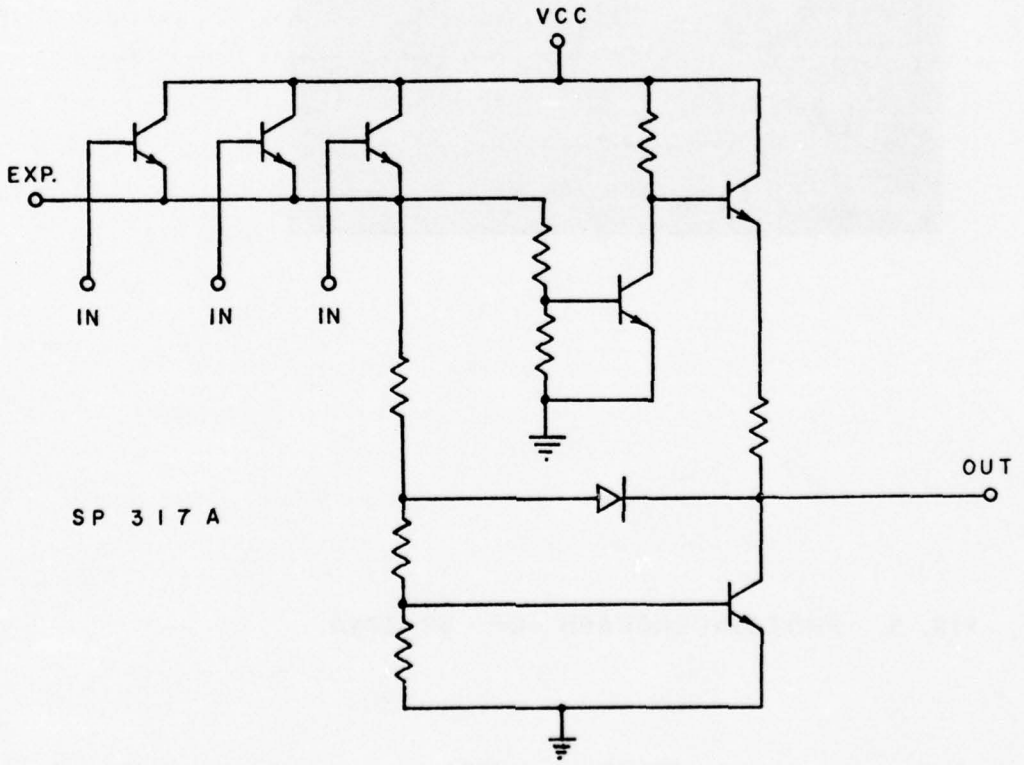
SP 300A



SP 333 / 334 / 374

FIG. 4 SIGNETICS UTILOGIC II/600 USING EFL





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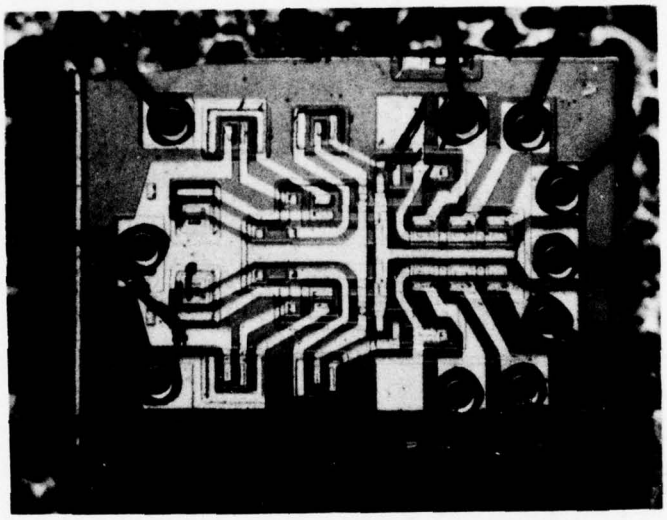


FIG. 5 PHOTOMICROGRAPH OF SP 374A

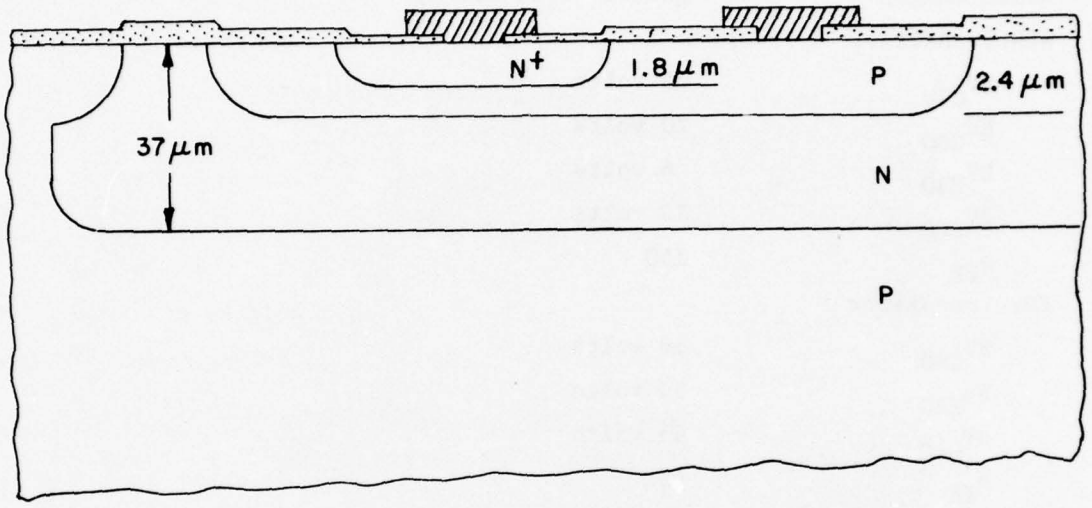
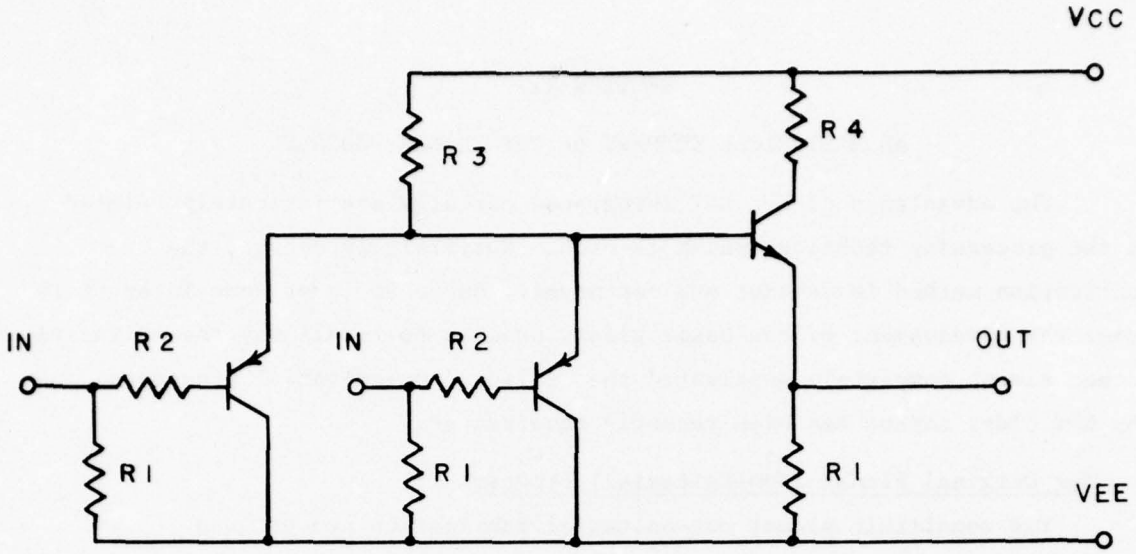


FIG. 6 TYPICAL UTILOGIC CROSS SECTION

and logic diagram are shown in Fig. 7. The input stages are PNP emitter followers which perform the AND function. The output transistor forms an NPN emitter follower buffer stage. Characteristics are as follows (4):

Propagation delay	2-4 ns
Gate dissipation	30-35 mW plus 5 mW per fan-out
Binary count rate	30 MHz
Logic swing	3 volts
Noise margin	greater than 500 mV
NPN Transistor	
BV_{CSO}	65 volts
BV_{CBO}	20 volts
BV_{EBO}	6 volts
BV_{CEO}	12 volts
h_{FE}	150
PNP Transistor	
BV_{CBO}	68 volts
BV_{EBO}	50 volts
BV_{CEO}	65 volts
h_{FE}	40
Substrate	p-type, 5 ohm-cm
Epitaxial layer	0.6 ohm-cm, 5.5 μm
Base diffusion	150 ohms per square, 2.4 μm
Emitter diffusion	3 ohms per square, 1.8 μm
Die size	46 x 46 mils
Component density	18,000 parts per square inch

Fairchild considers Complementary Transistor Micro-Logic to be a high speed logic family. When emitter followers are used, customers are cautioned about the possibility of parasitic oscillations.



VCC = 4.5 V. ± 10%
VEE = −2.0 V. ± 10%

TYPICAL SCHEMATIC OF ONE 2-INPUT AND GATE (POS. LOGIC)

TOP VIEW

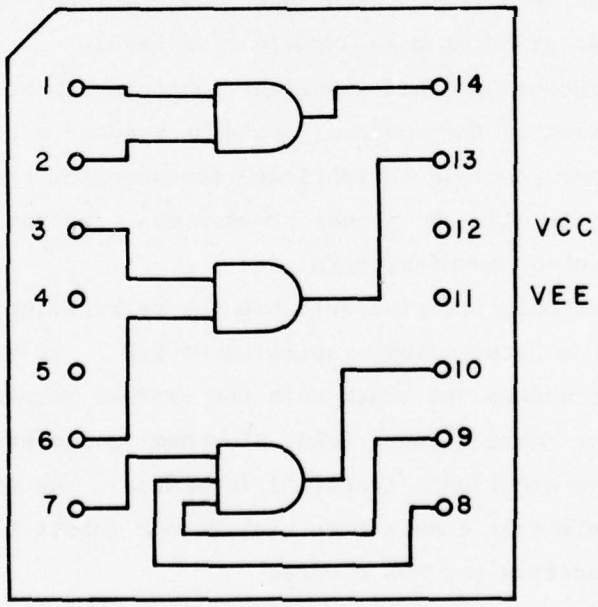


FIG. 7 FAIRCHILD CTμL − 953 AND GATE

SECTION III

AN HISTORICAL SUMMARY OF THE PLANAR PROCESS

The advantages of EFL LSI integrated circuits are intimately related to the processing technique which is used. Surprisingly enough, the fabrication method is neither new nor novel. Hence it is of some interest to trace the development of the basic planar process to recall why the epitaxial method almost completely supplanted the earlier, non-epitaxial processes, and why the older method has been recently resurrected.

A. The Original Planar (Non-Epitaxial) Process

The monolithic planar non-epitaxial fabrication process was introduced in 1960 by Fairchild Semiconductor. It had certain advantages over the alloy, mesa, and other processes which were used at that time to manufacture discrete transistors. Among these were careful control of impurity profiles, control of geometries, top contact availability, use of thermally grown oxide, and most important, passivation of the surface of the device, especially junction regions. Junctions in other technologies were exposed to the ambient. The high electric fields attracted foreign particles and led to reliability problems. With junctions completely sealed by silicon dioxide these problems were largely eliminated.

The planar process also had important economic advantages. The SiO_2 layer, besides passivating the surface, could be used as a diffusion mask. Furthermore, it became possible to fabricate thousands of transistors simultaneously. All in all, the planar process was a technological breakthrough for semiconductor manufacturers.

Silicon is the only material suitable for fabrication by the planar process because of the outstanding properties of SiO_2. It forms a dense, impervious layer which does not crack over the extreme temperature ranges encountered in device fabrication. Gold, aluminum, and other metals adhere well to it. It is an excellent electrical insulator. The dielectric losses are low, and the dielectric constant is high enough (about 4) to allow the construction of capacitors and MOS devices.

It was quickly discovered that multiple transistors, diodes, and resistors could be fabricated on the same chip if isolation between elements

was used. Thus the integrated circuit was born. To accomplish the necessary isolation reverse-biased junctions were resorted to. A triple diffused scheme, in which the collectors, bases, and emitters of NPN transistors were sequentially diffused into a p-type substrate, came to be one of the standard processes.

The details of one early process (5) are repeated here to show the similarity with modern methods. Details are shown in Figs. 8 and 9.

Starting material - 3/4 inch, 5 mil silicon wafer, p-type, 10 ohm-cm

Step 1 Clean Substrate

2 Thermal Oxidation
Oxide Mask
950°C Steam

3 Photoresist Coating

4 Pattern Formation
Artwork 50-100X
0.001" - 0.0001"
N-layer Pattern
Expose, Develop

5 Etch, HF
Wash, Dry

6 Diffusion, 1200°C ± 1°C
Sb, As, Bi (Gaseous)
Resistor 5000 ohms/square ± 20%
Transistor Collector

7 Etch, HF
Oxide Mask Removal

8 Thermal Oxidation
Oxide Mask
950°C Steam

9 Photoresist Coating

10 Pattern Formation
P-layer Pattern
Transistor Base
Expose, Develop

11 Etch, HF
Wash, Dry

12 Diffusion, 1200°C
Al, B, In (Gaseous)
Junction Capacitor .01-0.2 μF/square cm
Polarized 6-200 v d-c
Voltage Sensitive

13 Etch, HF
Oxide Mask Removal

14 Thermal Oxidation
Oxide Mask
950°C Steam

15 Photoresist Coating

16 Pattern Formation
N^+-layer Pattern
Transistor Emitter
Contact Areas

17 Etch, HF
Wash, Dry

18 Diffusion, 1200°C
Sb, As, Bi (Gaseous)

19 Etch, HF
Oxide Mask Removal

20 Thermal Oxidation
Oxide Protective Surface
950°C Steam

21 Photoresist Coating

22 Pattern Formation
Protective Layer
Connection Areas
Expose, Develop

23 Metallize, Vacuum Deposition

24 Interconnection Pattern
Aluminum

25 Wafer Shaping
Sawing, Ultrasonic Cutting
Etching, Scribing

26 Mounting Circuit Die
Alloying to Header

27 Lead Attachment
Thermal Compression Bonding
Header to Wafer Contacts
Gold Wire

28 Cover Attachment
Welding

This process includes 3 diffusions, 4 oxidations and 5 masks.

The first planar process, relatively simple by today's standards, allowed much higher packing densities than the mesa, thin film, or other contemporary techniques. Device parameters within a single chip could be closely matched. This meant that resistor ratios could be rigidly controlled and that high gain differential amplifiers were possible. Temperature tracking no longer posed a problem because all the devices on one chip were in good thermal contact with each other. Great strides were made in the evolution of circuits that were cheaper, more reliable, and of ever-increasing complexity and sophistication.

The characteristics of some of these early integrated circuits are of some interest. The following specifications have been taken from an early Fairchild Semiconductor publication (6).

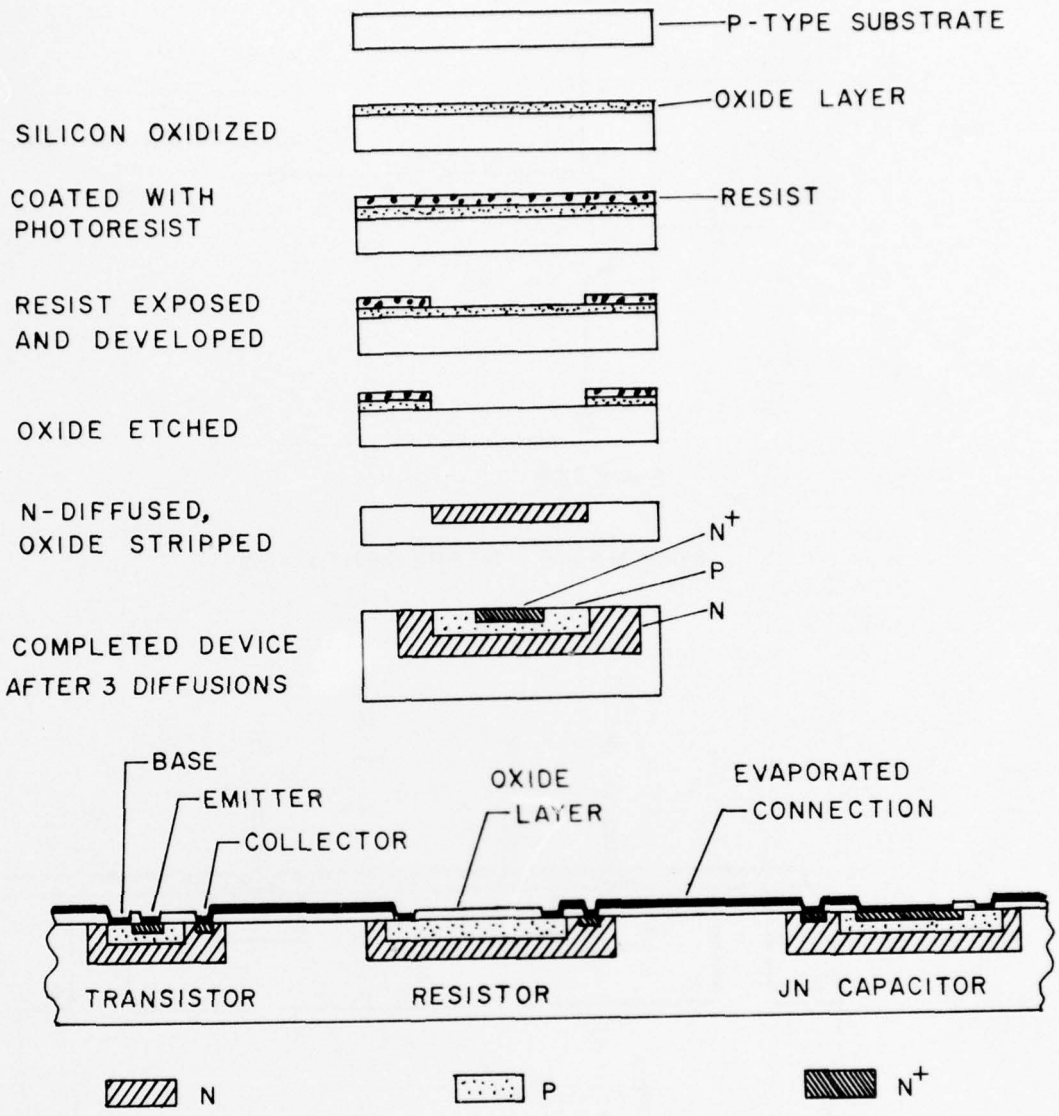
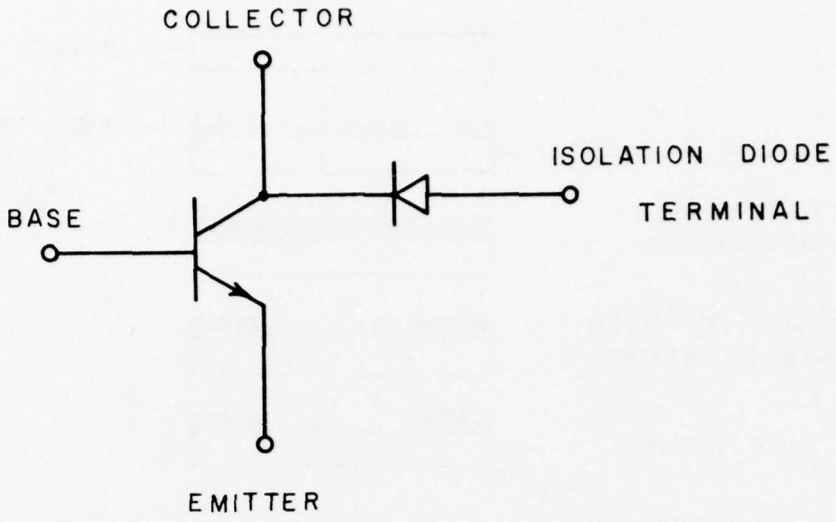
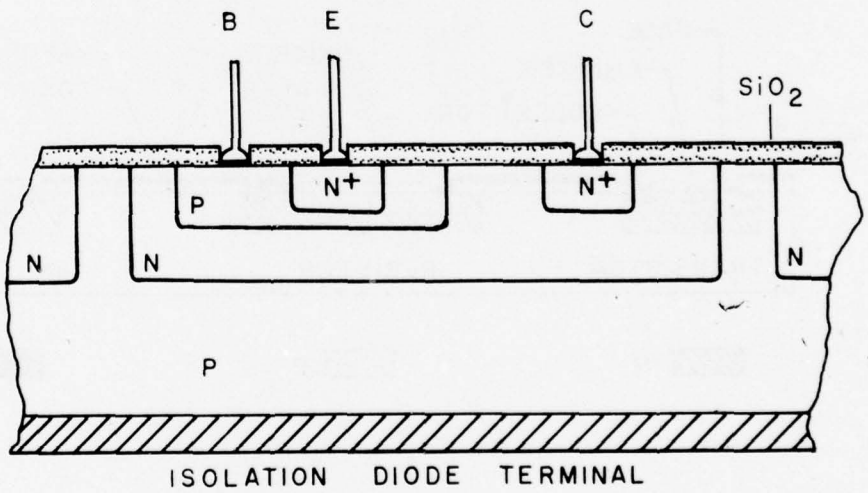


FIG. 8 MAJOR PROCESS STEPS IN NON-EPITAXIAL, PLANAR FABRICATION WITH TYPICAL MONOLITHIC CROSS SECTIONS



SCHEMATIC REPRESENTATION



CROSS SECTION

FIG. 9 ISOLATION REGION MODEL

Resistors (1500 ohms, nominal value)

Resistor tolerances	± 25% at 25°C
Resistor match	5% for a 6:1 ratio
Temperature coefficient	0.2% from 25°C to 125°C
	0.06% from -55°C to 25°C
Temperature tracking	0.005%/°C
Breakdown voltage	12 volts, resistor to substrate, 10th percentile
Shunt capacitance	20 pF
Sheet resistance	170 ohms per square

Diodes

Breakdown voltage	12 volts, 10th percentile, 10 μA
Forward voltage	0.85 volts at 3 mA
Leakage current	10 nA at -10 volts
Reverse recovery time	7 ns at 10 mA forward and reverse current
Junction capacitance	3.2 pF at 0 volts

Transistors

h_{FE}	80 at 3 mA
V_{BE} (sat)	0.75 at 3 mA
V_{CE} (sat)	0.25 at 3 mA
h_{fe}	3.8 at 100 MHz
BV_{CSO}	12 volts at 10th percentile
BV_{CBO}	12 volts at 10th percentile
BV_{EBO}	5 volts at 10th percentile
h_{fe} Match	20%
V_{BE} Match	5 mV
V_{BE} temp. coeff.	-1.8 mV/°C

Integrated Circuits

Propagation delay	40 ns
Gate dissipation	2 mW
Fan-out	5
Component density	26,000 per square inch

B. Disadvantages of the Non-Epitaxial Planar Process

In the mid 1960's the original planar process was all but abandoned in favor of the present epitaxial buried-layer bipolar process. What were the reasons that led to this abrupt change? They were related to difficulties in process control and to less than optimum electrical performance.

The problems in process control were due to the need to superimpose three different diffusions, each one being required to overcompensate and invert the existing impurity type. A first, deep collector diffusion could be well controlled. During the following p-type base diffusion the junction was formed where the boron concentration equaled the varying background collector concentration. Since the collector concentration ranged exponentially with distance (as did the base concentration) it was very difficult to control the exact depth of the collector-base junction. Consequently it was difficult to control the resistivity on the collector side of the junction (and on the base side). Similar problems were encountered with the emitter diffusion. In addition, the emitter needed to be very heavily doped, reaching or exceeding the solid solubility limit of the phosphorous impurity. This introduced strain, phase changes, anomalous diffusion, etc. The end result of all this was that reproducibility and yield suffered.

Electrical properties were degraded by the impurity profile of the triple diffused structure. In particular, the collector region was not optimized. The collector impurity concentration was highest close to the junction. This reduced the collector-base breakdown voltage and increased the collector-base capacitance. In addition, the resistance of the bulk collector material was high. This lead to high V_{CE} (sat), reducing logic swings and noise margins, and increasing circuit dissipation to intolerable levels for LSI applications.

A further problem concerns the parasitic PNP between base, collector, and substrate. The impurity gradient is such as to provide field-enhanced diffusion of minority holes injected into the n-type material from the p-diffused region. This produces a respectable current gain for this parasitic transistor. In fact, this current gain is essential for the proper operation of the PNP transistors in complementary emitter follower circuits. In TTL logic, this parasitic transistor action shunts the

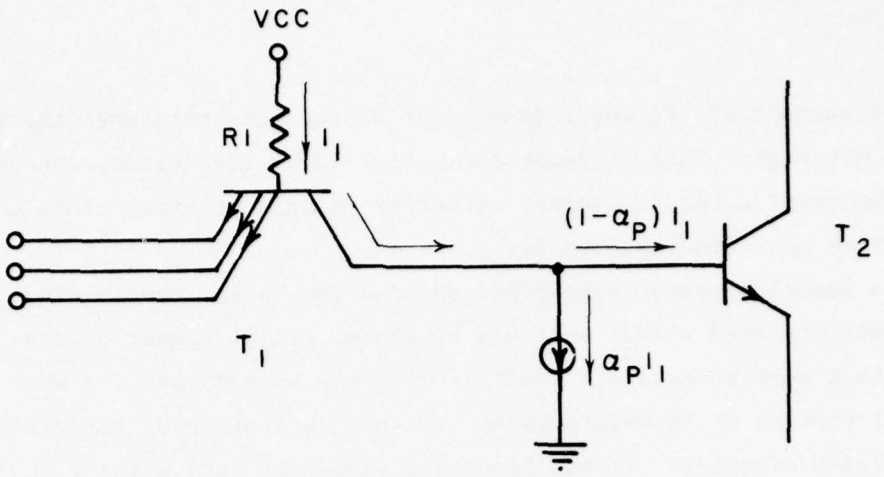
collector current of the input transistor to the substrate when the input emitters are high. This is depicted in Fig. 10 by the current source labeled $\alpha_P I_1$. The problem can be avoided either by using a Schottky clamp on T1 or by inserting an extra resistor R2.

As a result of these subtle but serious drawbacks, the original planar process was replaced almost entirely by the epitaxial planar process. It is assumed that most readers are familiar with the buried layer, planar epitaxial process as it exists today for the fabrication of saturating digital logic circuits. It has been used almost exclusively for the past 10 years. Recently, however, modifications of the original non-epitaxial process have appeared. We will now examine two of these modifications as produced by Western Electric and TRW, Inc.

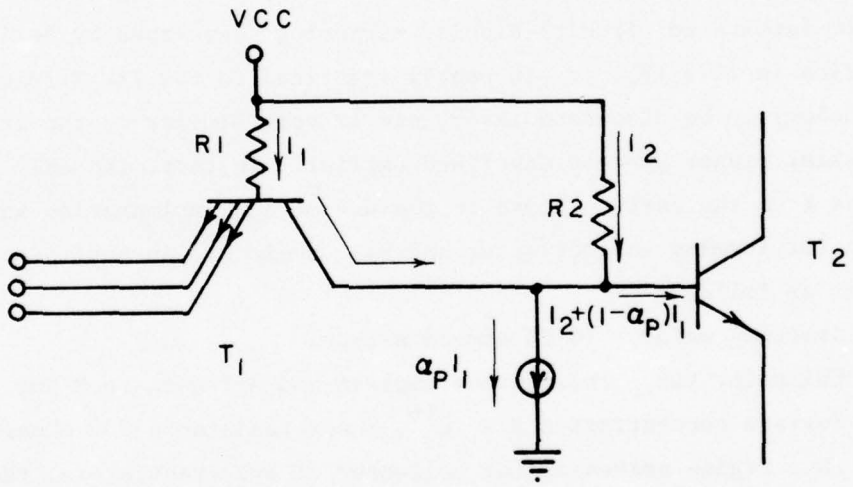
C. GIMIC-O, A Recent Non-Epitaxial Bipolar Fabrication Method

GIMIC-O (7) is a modification of the GIMIC (Guard-ring Isolated Monolithic Integrated Circuit) bipolar technology developed by Bell Telephone Laboratories in 1972 (8). It is nearly identical to the TRW Triple Diffused EFL technology to be discussed later, and is very similar to the original non-epitaxial planar process described earlier. In fact, the only significant difference from the early process is the use of ion implantation instead of diffusion for forming the collector and base regions. An outline of the process is as follows:

1. Starting wafer - 10-20 ohm-cm p-type
2. Collector tub - Phosphorous implant and drive-in to 8 μm. Surface concentration 3×10^{16}, sheet resistance 700 ohms/square. This region serves as the collector of NPN transistors, the base for PNP transistors, n-type resistors, and as the n-side of Schottky diodes.
3. Base region implant - A two-step boron implant 1.2 μm deep. Surface concentration 1×10^{18}, sheet resistance 600 ohms/square.
4. Emitter diffusion - Standard phosphorous diffusion, 0.6 μm deep, 25 ohms/square. Used for emitters and crossunders.
5. Oxide stripping and redeposition - this facilitates metal coverage.



BASE CURRENT FOR T_2 SHUNTED TO SUBSTRATE, PREVENTING T_2 FROM SATURATING.



$\alpha_P \geq 0.9$

R2 PROVIDES SUFFICIENT CURRENT ALLOWING OVERDRIVE CURRENT TO BASE OF T_2. T_2 CAN NOW SATURATE.

FIG. 10 PROBLEM ENCOUNTERED WITH PLANAR PRODUCED SATURATING LOGIC AND ITS REMEDY.

Western Electric continues the process to form beam-lead Schottky barrier devices. A standard process would continue after Step 5 with pre-ohmic etch, metallization, glassivation, and pad etch. As such, it would require 6 masks, 2 ion implants, one diffusion, and 5 thermal or deposited oxides. The processing steps are shown in Fig. 11.

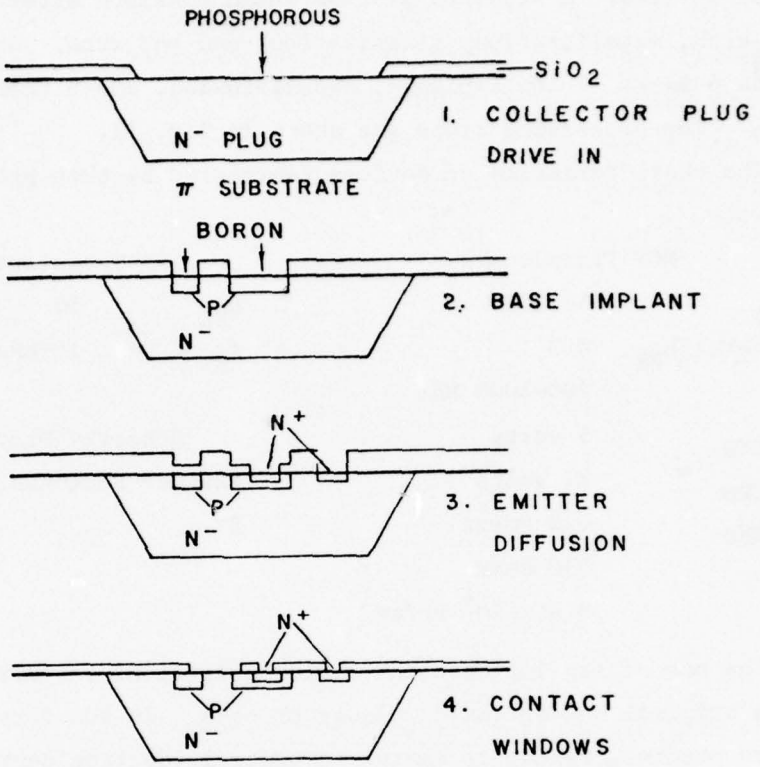
The characteristics of devices fabricated by this process are as follows:

NPN Transistors		PNP Transistors	
h_{FE}	50-150	h_{FE}	10
Inverse h_{FE}	0.3	f_T	15 MHz
f_T	700-1000 MHz		
BV_{CEO}	9 volts	Schottky Diode	
BV_{CBO}	27 volts	Barrier Potential	0.85 volts
BV_{EBO}	6.2 volts	BV	27 volts
R_C	550 ohms		
C_B	3.4×10^4 pF/cm^2		

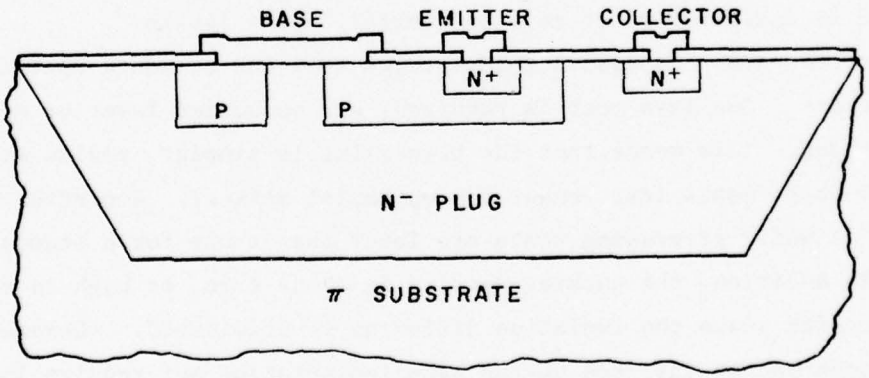
The use of ion implantation avoids several of the difficulties inherent in the original non-epitaxial planar process. In the first place, the method is more precise, making it easier to control junction depths and resistivities. By tailoring the impurity profiles it is possible to adjust junction breakdown voltages and capacitances. If Schottky barrier diodes are employed it is essential to be able to control doping levels.

The process also has distinct advantages over the standard epitaxial bipolar process. One less mask is required, and no buried layer or epitaxial layer is needed. This means that the processing is simpler, yields are higher, and photo-masks last longer (no epitaxial spikes). According to reference (7) wafer processing costs are lower than those for a standard PMOS process. In addition, the packing density is about twice as high as standard bipolar circuits since the isolation diffusion is eliminated. (Channel stops or guard bands can be inserted during base implantation but require less area than the deep isolation diffusion).

Although the method is suitable for nearly any logic family, it is presently being used primarily for low power Schottky clamped TTL circuits. The Schottky clamps eliminate the problem of bypassing current to the



PROCESS SEQUENCE FOR THE GIMIC-O STRUCTURE



CROSS SECTION OF A SCHOTTKY CLAMPED GIMIC-O TRANSISTOR

FIG. 11

substrate by the parasitic PNP's since the collector junction of the NPN is never forward biased.

Gates with specifications the same as a standard TTL family can be made with a power delay product of 20 pJ at 1 mW. Internal gates with reduced logic swing operate at 2-5 pJ. An 8-bit parallel output shift register (70 equivalent gates) on a 110 x 110 mil chip with standard LTTL input and output specifications operates at 10 MHz and 45 mW.

The features of the GIMIC-O technology can be summarized as follows:

1. No buried layer
2. No epi layer
3. Ion implanted collector and base regions
4. Ion implanted resistors both N and P type
5. PNP transistors available
6. Schottky barrier diodes available
7. Simple processing
8. High packing density
9. High yields

D. Triple Diffused Process for Emitter Follower Logic

The triple diffused process has been utilized for several years at TRW as a simple method for producing custom, in-house integrated circuits. Its potential for low cost, high yield LSI circuits was the reason for recent renewed interest in this type of fabrication process. The technology will be discussed in much greater detail in later sections, but a brief summary will be given here to complete the present section. The triple diffused process is nearly identical to the GIMIC-O process just discussed. The difference is in the impurity profiles - much heavier doping levels are employed, and junction depths are somewhat shallower.

The fabrication sequence is summarized below.

1. Starting wafer - 0.8 ohm-cm, p-type
2. Collector implant and diffusion - 4.8 μm, 100 ohms/square
3. Base implant and diffusion - 2 μm, 125 ohm/square
4. Emitter diffusion - 1.5 μm, 7 ohms/square

The heavier doping precludes the use of Schottky clamps. Nevertheless TTL circuits can still be fabricated which avoid the current bypass problem

by adding another resistor as shown previously in Fig. 10. Complementary emitter follower logic fabricated by this process has achieved clock rates of 30 MHz, nominal stage delays of 7 ns, speed power products of 10 pJ, and packing densities of 33,000 gates per square inch. Even better performance is available from improved versions.

The strongest argument for this technology is that it is capable of producing LSI circuits of great complexity at reasonable cost. The key to meeting this objective is unusually high yields. TRW has been able to accomplish this by careful design, a well-controlled manufacturing process, and extreme care in making and using photomasks. As of this writing, no other company has been able to achieve such high yields by this process, although they do achieve yields which are considerably higher than normal for the IC industry. In the following sections, the triple diffused process will be critically examined to assess its potential as a viable LSI technology.

SECTION IV

TRIPLE DIFFUSED EMITTER FOLLOWER LOGIC

This section presents the details of triple diffused emitter follower logic as developed by TRW, Inc. Material for this and following sections is taken from various publications by TRW personnel (1, 9, 10, 11, 12) and the authors of this report gratefully acknowledge their help and cooperation.

A. Reasons for the Development of Triple Diffused Emitter Follower Logic

In the early 1970's an optimum technology for LSI implementation of digital circuits was required. The design criteria to be met included

1. High speed
2. High packing densities
3. High yields
4. Cost effectiveness.

There were arguments raised against the use of MOS and standard bipolar technologies. Epitaxial buried-layer bipolar devices have lower producibility and higher dissipation than MOS devices. On the other hand, MOS cannot deliver the high digital data rates (30 MHz) required. Triple diffused emitter follower logic meets these and other specifications. In this section it will be shown that this technology provides

1. High speed. Factors contributing to high speed are
   a. EFL is a non-saturating bipolar family
   b. EFL gate delays obey rules of RSS (RSS is root of the sum of the squares) summation instead of linear summation.
2. High packing densities, comparable to MOS. These are attributed to
   a. Smaller device dimensions
   b. Use of self-isolating resistors
   c. Combining circuit cells into smaller, electrically common regions.
3. Exceptionally high yields for LSI as compared to other technologies. Reasons for this include
   a. Process simplicity
   b. Close manufacturing tolerances
   c. Exceptional mask quality

d. Deep junctions which minimize defects

e. Low sensitivity to wafer defects.

4. Cost effectiveness. This is due to

a. Process simplicity

b. High yields.

B. The Triple Diffusion Process

The triple diffusion process evolved from the original planar process. As developed by TRW, it can be used to fabricate both NPN and PNP bipolar transistors and self-isolating resistors on the same substrate. The technology requires three impurity dopings and distributions done in sequence. A p-type silicon crystal is used as the substrate material. A list of major processing steps describing the technique is provided below. Figures 12 A and B illustrate significant process steps.

1. First oxidation
2. Collector photoresist
   Oxide etch
   Clean, grow thin oxide
3. Collector impurity ion implant, n-type
   Clean, anneal
4. Collector distribution diffusion
   Collector depth of 4.8 μm
   Sheet resistance of 100 ohms/square
5. Base photoresist
   Oxide etch
   Clean, grow thin oxide
6. Base impurity ion implant, p-type
   Clean
7. Base distribution diffusion
   Base depth of 2.0 μm
   Sheet resistance of 125 ohms/square
8. Emitter photoresist
   Oxide etch
9. Emitter thermal impurity deposition
   Emitter thermal impurity distribution

Depth of 1.5 μm

Sheet resistance of 7 ohms/square

10. Measure and thermally adjust Beta

    $\beta_{PNP} = 10$

11. Contact photoresist

    Etch, clean

    P-type contact deposition

12. Beta adjust

    $\beta_{NPN} = 35$

13. Metal deposition

    50 Å Ti and 17,000 Å Al

14. Metal photoresist

    Etch, clean

    Sinter

15. Passivation oxide

16. Passivation photoresist

    Etch, clean

17. Deposit back metal

    Alloy

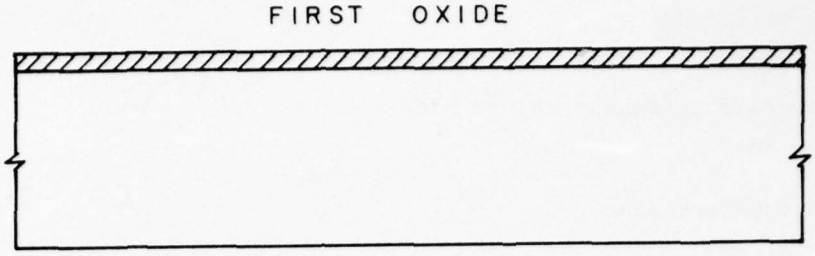
18. Functional probe test

19. Device characterization probe test

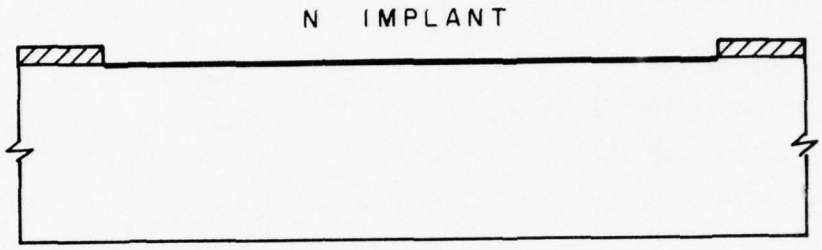
20. Saw wafer into chips

At this point, the LSI chips are ready for packaging.

Step 19 is used to determine uniformity between runs. The d-c parameters of the devices located around the periphery of each chip are measured. This is a 100% test on each wafer completing the process. Table 1 lists triple diffused electrical properties. In summary, the triple diffused process has 2 ion implants, 1 impurity deposition, 3 impurity diffusions, 4 oxide layers, and 5 masks (not counting final scratch protection).

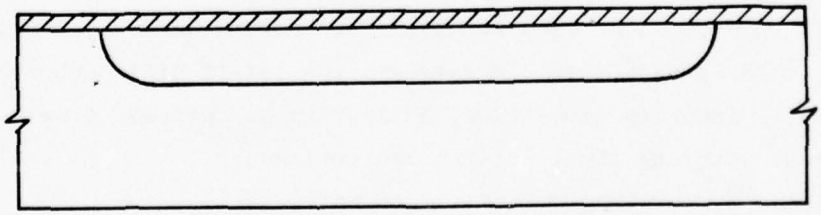


1. FIRST OXIDATION



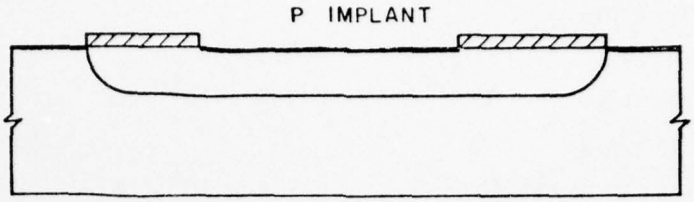
2. COLLECTOR PR AND IMPLANT

3. STRIP OXIDE

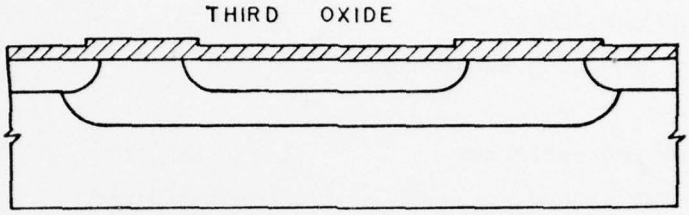


4. N-COLLECTOR DISTRIBUTION AND SECOND OXIDATION

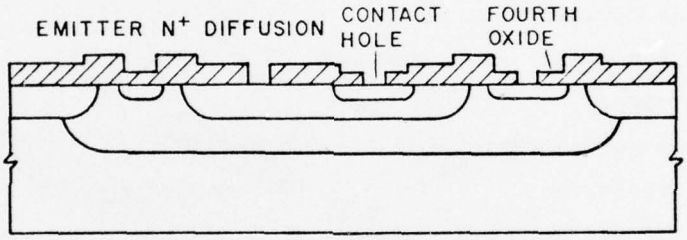
FIG. 12 A NON-EPITAXIAL TRIPLE DIFFUSION PROCESS



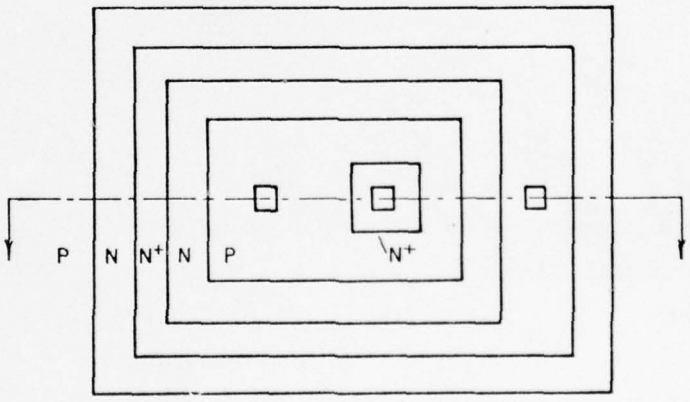
5. P BASE PR AND IMPLANT



6. P BASE DISTRIBUTION AND THIRD OXIDE



7. N^+ EMITTER DIFFUSION, FOURTH OXIDE AND CONTACT PR



AN NPN TRANSISTOR

FIG. 12 B

TABLE 1

Electrical Properties of the Triple Diffused Structure

Substrate (p-type)		
Resistivity		0.8 ohm-cm
Concentration		$2.5 \times 10^{16}/cm^3$
Collector (n-type)		
Surface concentration		$9.6 \times 10^{17}/cm^3$
Sheet resistance		100 ohms/square
Junction depth		4.8 μm
Average mobility		386 cm^2/v-s
Average mobility under base		441 cm^2/v-s
Base (p-type)		
Surface concentration		$1.2 \times 10^{19}/cm^3$
Sheet resistance		124 ohms/square
Junction depth		2.0 μm
Average mobility		54 cm^2/v-s
Average mobility under emitter		39.6 cm^2/v-s
Emitter (n^+-type)		
Surface concentration		$6.5 \times 10^{20}/cm^3$
Sheet resistance		7 ohms/square
Junction depth		1.5 μm
Average mobility		47 cm^2/v-s
Alpha Cut-off Frequency		
NPN		143 MHz
PNP		51 MHz
Junction Capacitances		
E to B	@ -3 V	0.42 pF/mil^2
B to C	@ -3 V	0.25 pF/mil^2
C to Substrate	@ -3 V	0.08 pF/mil^2
Diffused Resistor Values		
Emitter		7 ohms/square
Base		124 ohms/square
Collector		100 ohms/square
Pinched collector region		472 ohms/square
Pinched base region		18K ohms/square

In the triple diffusion process, the P-type substrate is actually the PNP transistor collector region, as illustrated in Fig. 13. For this reason, the PNP transistors can be used only in the common collector configuration. These transistors are vertical devices and their collectors are the common substrate. It is these PNP transistors which act to divert the base overdrive current when saturating logic is employed. If the PNP transistors were not present, most of the base overdrive current would flow into the base of the following transistor, as described in Section II of this report. This inability of planar fabricated circuits to drive saturating logic was a major argument against the process.

The simultaneous fabrication of both PNP and NPN transistors on a common substrate with the NPN collector and PNP base sharing a common region is a space-saving feature. Coalescing of transistor structures is not restricted with the triple diffused process. Since strong vertical diffusion gradients are used in the triple diffusion process, transistor action is restricted to the immediate vicinity of the device. Therefore there is reduced lateral PNP transistor action, resulting in closer inter-device spacing. This results in higher device packing densities. In technologies not using the substrate for an active region of their PNPN transistors, guard ring techniques are necessary. Therefore, these technologies have lower packing densities than the triple diffused structure.

C. Modelling the Triple Diffused Structure

Any discussion of a technology fabrication procedure would be incomplete without briefly considering a model for the structure. The model used is a modification of an Ebers-Moll model and is a good approximation up to frequencies of 0.30 f_α, where f_α is the alpha cut-off frequency of the device. The approximations given by the model have maximum errors of 10%. Figures 14 A and B depict the NPNP and PNP transistor models, respectively. Junction diodes are described by the diode equation

$$I(q/kT) = I_o(e^{qv/kT}-1),$$

while junction capacitances are governed by

$$C = C_o\left(1 - \frac{V}{V_{CNT}}\right)^{-0.4} + \tau I(q/kT),$$

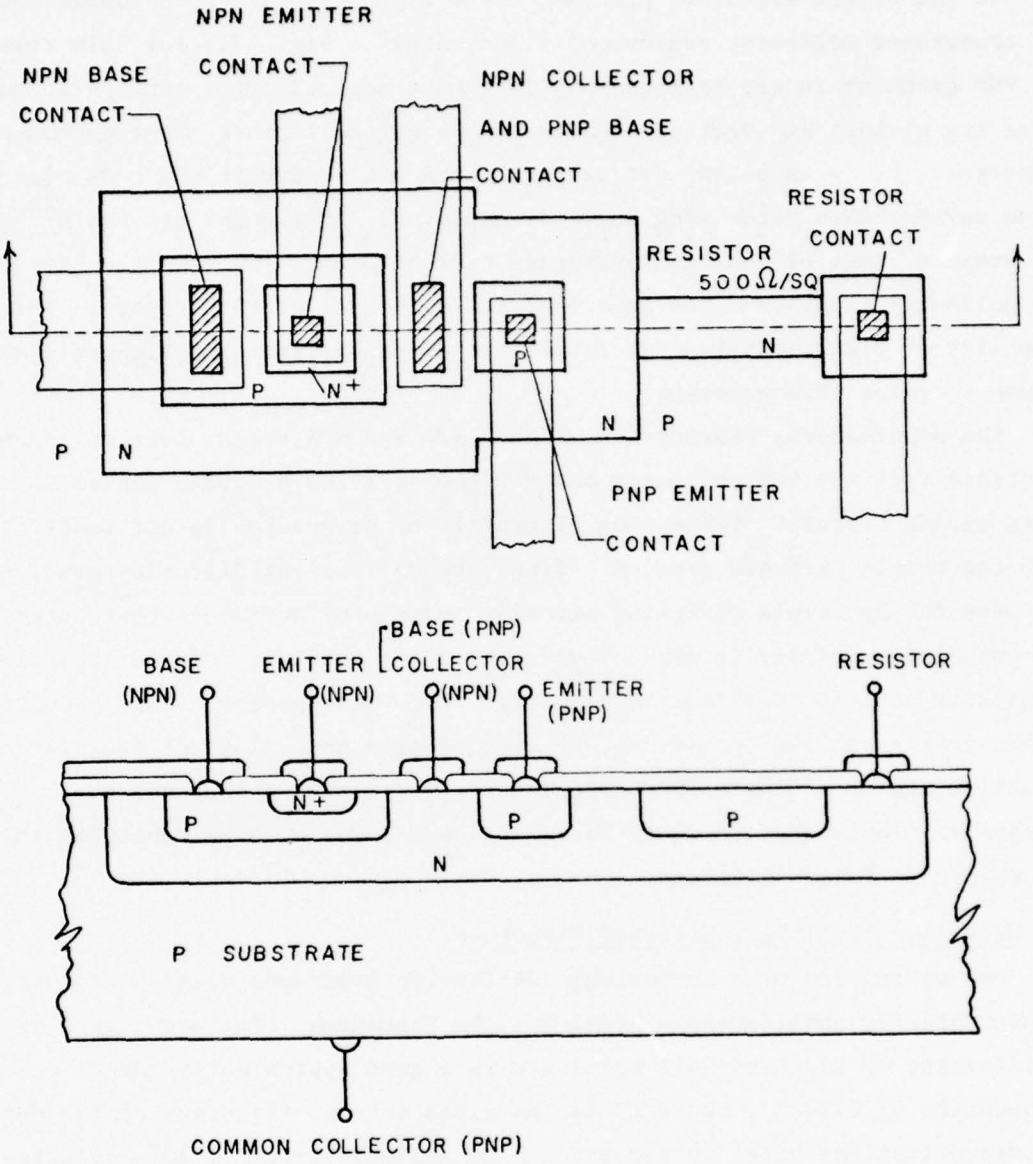
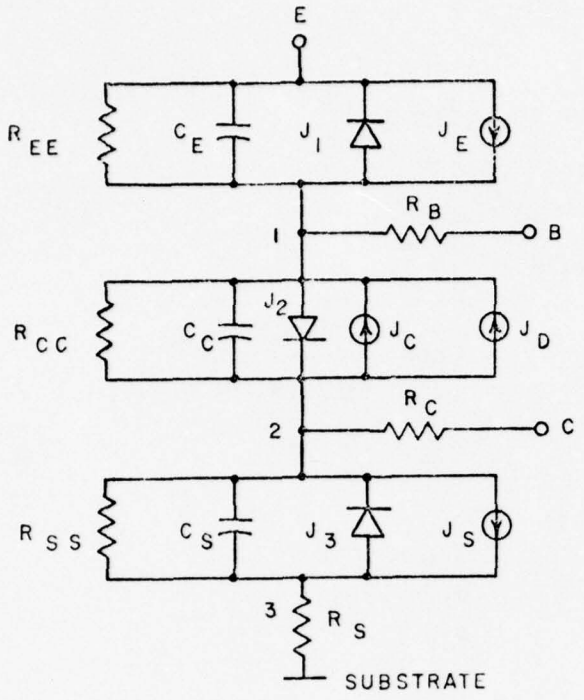


FIG. 13 TRIPLE DIFFUSED EFL COALESCING STRUCTURE



$R_{EE} = R_{CC} = R_{SS} = 10^4$K

$R_B = .15$K
$R_C = .125$K
$R_S = .2$K

$I_{01} = 4.541 \times 10^{-14}$ mA
$I_{02} = 1.441 \times 10^{-13}$ mA
$I_{03} = 3.113 \times 10^{-13}$ mA

$\tau_{EB} = 1.27$ ns
$\tau_{BC} = 4.0$ ns
$\tau_{CS} = 40.0$ ns

$C_{OE} = .46$ pF
$C_{OC} = .65$ pF
$C_{OS} = .54$ pF

$V_{EB} = .931$ V
$V_{BC} = .931$ V
$V_{CS} = .88$ V

$\alpha_N = .967$
$\alpha_P = .75$
$\alpha_{IN} = .2$
$\alpha_{IP} = .01$

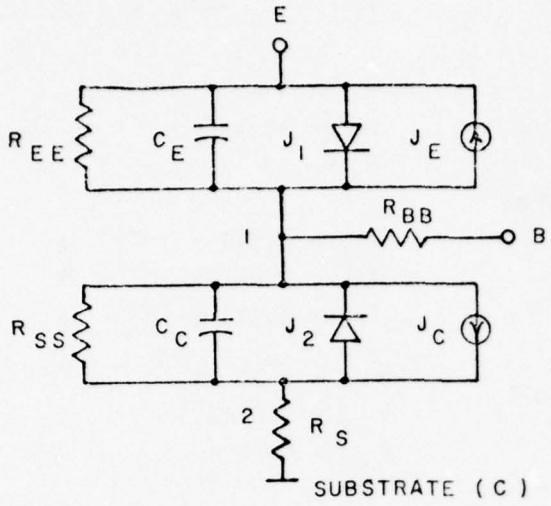
Temperature Coefficients

R_B, R_C, R_S: +.4%/°C

β_N, β_P: +.8%/°C

τ_{EB}, τ_{BC}, τ_{CS}: -.027%/°C

FIG. 14 A NPNP TRANSISTOR MODEL



$R_{EE} = 10^4 K$
$R_{SS} = 10^4 K$

$R_B = .15K$
$R_S = .2K$

τ_{EB} = 4.0 ns, for NPN
= 2.0 ns, for NPN

$C_{OE} = .65$ pF
$C_{OC} = .25$ pF

$V_{EB} = .931$ V
$\alpha_P = .95$
$\alpha_{IP} = .01$

Temperature Coefficients

R_B, R_S:	+.4%/°C
β_P:	+.8%/°C
τ_{EB}:	-.027%/°C

FIG. 14 B PNP TRANSISTOR MODEL

where

I = junction current in the forward direction

V = voltage across a forward-biased junction

V_{CNT} = junction constant potential

I_o = junction saturation current

C_o = zero bias junction capacitance

τ = storage time constant $(2\pi f_\alpha)^{-1}$

I_o is determined by measured values of NPNP voltages at

0.5 mA: $V_{BE_1} = 0.78$ V, $V_{BE_2} = 0.75$ V, $V_{BE_3} = 0.73$ V.

D. Characteristics of Emitter Follower Logic Circuits

In Table 2, the operating parameters for EFL are listed and compared against standard TTL. Note that the speed power product of the triple diffused EFL is comparatively low. This can be attributed mainly to the lower transition time between states required by the non-saturating logic. Notice that the TTL requires 60-97 process steps and from 7 to 11 masks while triple diffused EFL requires 65 steps and only 5 masks. This gives an indication that the triple diffused EFL may have higher reliability and integrity than TTL devices produced by standard bipolar methods. Because process complexity is low for this bipolar technology, it is seen that EFL can be more cost effective than TTL on a circuit for circuit basis of comparison. These apparent attributes, in conjunction with higher device densities attainable than when using epitaxial construction, allow triple diffused EFL to be considered as an LSI technology.

Here, it is timely to compare families of LSI technologies in order to visualize how triple diffused EFL weighs with other families, both MOS and bipolar as shown in Table 3 (13). Although OAT processes and epitaxial ECL have high operating speeds while maintaining a low delay power product, triple diffused EFL exhibits a circuit density which exceeds that of both OAT and ECL by an order of magnitude. Likewise, the speed of 3D-EFL exceeds that of most MOS devices. These characteristics point out the advantages of EFL as an LSI technology.

E. Triple Diffused LSI Defect History

Perhaps the most important consideration in choosing a technology to implement LSI is the ability of the technology to suppress physical defects

TABLE 2

	3D-EFL	STANDARD TTL
Nominal Stage delay (ns)	7	8
Dissipation, static and dynamic @ 1 MHz (mW)	1.5	7.5
Speed power product (pJ)	10 (1 MHz) 15 (20 MHz)	60
Noise immunity (volts)	0.25	0.4
Repetition rate (MHz)	30	20-25
V_{CC} (typical, volts)	5.3	5
Signal swing (volts)	0.2 - 1.2	0 - 3.4
Number of masks (critical steps)	5	7-11
Process steps	65	60-97

TABLE 3

LSI Technology Comparisons

	Speed	Circuit Density	Delay x Power
Bipolar			
Triple Diffused EFL	30 MHz	20,000 Devices/Chip	10 pJ
Epitaxial ECL	250 MHz	5,000 Devices/Chip	2 - 5 pJ
OAT Process	1000 MHz	2,000 Devices/Chip	1 - 2 pJ
MOS			
PMOS	1 MHz	8,000 Devices/Chip	200 pJ
CMOS	5 MHz	3,000 Devices/Chip	50 pJ
CCD	5 MHz	100,000 Devices/Chip	0.1 pJ

which contribute to loss of yield. The majority of defects found in integrated circuits are point defects which occur in the preparation of photo masks and during the photoresist contact printing steps in processing. To minimize the density of point defects TRW maintains rigid controls during mask fabrication. Great care is exercised also when using the photo masks. With the proposed use of projection printing, not only is mask deterioration reduced, but greater resolution can be achieved. As a side-effect, the reduced mask wear also prolongs the life of masks and reduces production costs. Assuming that most yield losses occur because of mask defects, the extra care in manufacturing masks, the absence of epitaxial spikes which degrade masks, and the use of projection printing will all contribute to high yield.

In order to better appreciate the progression of triple diffused LSI along its learning curve it is instructive to observe its defect history as a technology. A paper published by A. G. F. Dingwall (14) shows the evolution of an index, D_o which is defined as the number of defects per cm^2. The development of the index is based on statistical distribution arguments which will not be considered in this report. The defect index is a variable used to calculate yield. This yield is defined as

$$\text{YIELD} = \left(1 + \frac{D_o A}{3}\right)^{-3},$$

where A is the chip area in cm^2.

Figure 15 is a plot of triple diffused LSI yield as a function of chip area and production year. An upper bound of yield is defined by the curve corresponding to $D_o = 1$, while the lower bound is determined by $D_o = 20$.

There is a tendency for the defect density to decrease as time increases, i.e., yields increase as a technology proceeds down its learning curve. A tabulation of approximate values of D_o for emitter follower logic, based on Fig. 15 is

D_o	Year
10	1972
5	1973
3	1974.

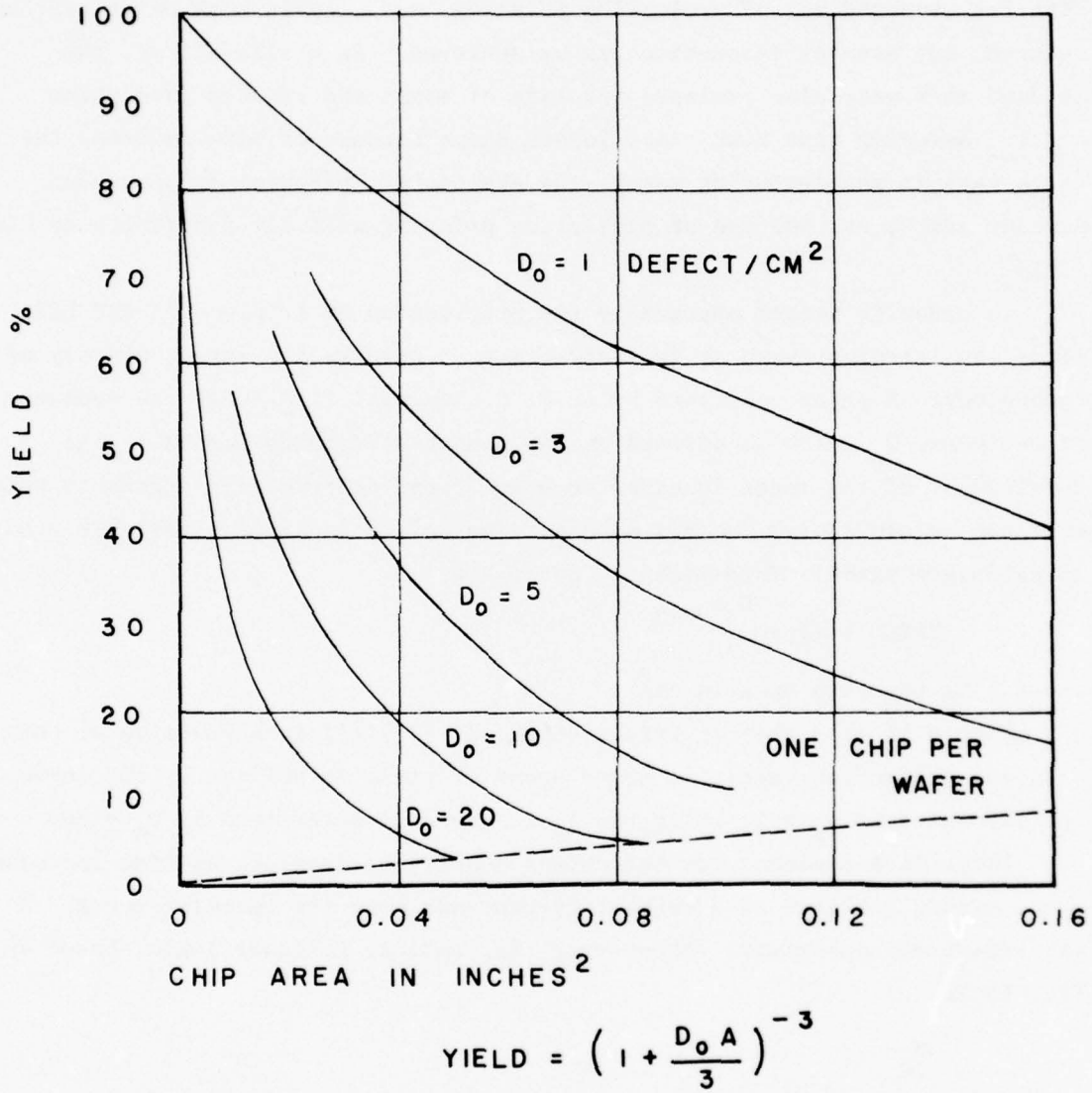


FIG. 15 TRIPLE DIFFUSED LSI YIELD

The yield describes wafer probe yield. It is estimated that the overall yield will decrease by an additional 50% after dicing, packaging, and final testing.

TRW has achieved yields of 80% on circuits measuring about 150 x 150 mils, and 25% on circuits of 315 x 351 mils. In 1975 Motorola produced some EFL circuits with the 3D process. At first, yields were disappointingly low, but improved as processing steps were optimized. When EFL was finally discontinued, yields were quite good, but not as good as TRW's. Western Electric, using the GIMIC-0 process has also achieved good yields with Schottky barrier TTL, but again not as high as TRW. This is a crucial issue, since 3D EFL is only cost-effective if the yields are high. TRW appears to have achieved unusually high yields by carefully controlling the process and by exceptional control of mask quality.

F. Radiation Effects

Triple diffused EFL has shown good hardness against radiation, including

a. Transient ionizing radiation
b. Neutron radiation
c. Cobalt - 60 ionizing radiation.

The two important factors which contribute to this radiation hardness are its structure and circuit form.

The triple diffused structure promotes an immunity to surface effects of ionizing radiation. Surface effects do not perturb a large percentage of resistors because they are buried, pinched collector devices. Because the base region has a relatively high surface concentration ($1.2 \times 10^{19}/cm^3$), the probability of surface inversion decreases greatly. Likewise, the 4,000 Å oxide would require an impressed voltage exceeding 100 V to cause inversion. Finally the heavily doped field guard rings around transistor and resistor contacts contribute to reduce the effects of surface radiation.

Emitter follower logic is itself tolerant to radiation. Because cascaded emitter followers provide sufficient gain to overcome the allowable beta degradation of 2 for PNP's and 3 for NPN transistors the circuit form is considered to be radiation hardened. These figures represent the maximum allowable beta degradations before the onset of logic margin loss.

The combining of emitter follower logic with the triple diffusion fabrication process enhances the radiation tolerance of the technology over the tolerances of the logic family and process structure considered individually above. Photocurrents generated by the incident transient radiation are bypassed to the substrate by the PNP parasitic transistor as discussed in Section III. Peak values of this photocurrent are reduced because the planar construction has a higher parasitic spreading resistance, as compared to buried-layer epitaxial devices. The combined effect of the substrate current sink caused by the parasitic PNP transistor and large series spreading resistance of the triple diffused EFL technology reduce the peak value of photocurrent and minimize surface inversion. For these reasons, the technology is considered as being radiation hardened. Table 4 shows radiation test results for random triple diffused EFL circuit geometries.

G. Future Developments in Triple Diffused Emitter Follower Logic

It has been stated that mask accuracy and care are paramount in the reduction of point defects associated with the triple diffusion process. The contact printing technique currently being used in this fabrication process allows for average spacings of about 4 micrometers. If closer spacings are required, then projection printing must be employed. Projection alignment printing could give good resolution with spacings as close as 1 micrometer. For this increased resolution, the price to be paid would include very critical exposure control using a positive photoresist process. One of the greatest advantages to be gained with the projection printing process is the extension of mask life. Since contact photoresist printing causes rapid mask deterioration, masks must be remade often to reduce point defects which occur as the mask degenerates.

The consequences of a 4 to 1 reduction in device geometry must now be considered. The spacing reduction would allow a four-fold decrease in junction area which would cause a corresponding decrease in junction capacitance. The reduction of junction capacitance would promote a decrease in the speed power product thereby increasing the figure of merit of the circuit.

Since devices would be closer together, junction depths must be decreased. This is so, since the lateral or sideways diffusion is dependent

TABLE 4

Radiation Test Results*

Cobalt - 60 (Co^{60}) Ionizing Radiation	
No loss of logic functions	$4x10^{7}$ rad(Si)
Max. operating frequency is 5-10% higher than original frequency.	
Beta degradation is 3 for PNP, 13 for NPN.	
Transient Ionizing Radiation	
Logic errors start to occur.	$4x10^{8}$ rad(Si)/sec.
Cessation of functions during irradiation Outputs are saturated at ground state.	$5x10^{9}$ rad(Si)/sec.
Output saturation persists for about one second after radiation burst before return to normal operation.	$9x10^{10}$ rad(Si)/sec.
Neutron Irradiation	
Operation normal Max. frequency is 30% higher than normal, due to reduced storage time constant.	10^{14} nvt
Operating circuit ceases to function. Operation can be returned to normal by damage annealing at 150°C for 24 hours.	$2x10^{15}$ nvt

*These radiation test results are somewhat pessimistic because no attempt was made to use radiation hardened circuit configurations. Such a configuration would tend to balance the effects of the radiation induced photocurrents.

on vertical diffusion distance. In order to facilitate the smaller junction depths and to enhance device characteristics, lighter doping levels must be used. The cumulative effect of lowering doping densities would be to further reduce the capacitance per unit area and to increase carrier mobilities within active regions. There is a serious potential drawback. One of the greatest influencing factors promoting the radiation hardness of present triple diffused EFL is the use of high doping levels. Should these levels be reduced it is possible that the future circuits may fail to be adequately hardened to ionizing radiation and that surface inversion will become a problem.

Comparisons between the current triple diffused LSI and the advanced shallower diffused structures are shown in Table 5. Types A and B are shallower diffused structures for the same process but at either end of the variation range. Notice the improvement of parameters such as the higher average mobilities under the emitter and base, higher alpha cut-off frequency, reduced junction capacitances, and resistors with higher sheet resistances.

By combining smaller lateral geometry with reduced diffusion profiles, a speed power product improvement by a factor of 6 and a four-fold increase in device density can be realized. This is shown in Table 6 where the present triple diffused structure is compared against a half-size advanced structure.

TABLE 5

Comparison between present 3D-LSI and Future (Advanced) 3D-LSI

	Present	A	B
Substrate (p-type)			
Resistivity (ohm-cm)	0.8	4.0	4.0
Concentration (/cm^3)	2.5×10^{16}	3.5×10^{15}	3.5×10^{15}
Collector (n-type)			
Surface concentration (/cm^3)	9.6×10^{17}	7.5×10^{16}	7.2×10^{16}
Sheet resistivity (ohms/sq)	100	750	900
Junction depth (μm)	4.8	3.5	3.0
Avg. mobility (cm^2/v-s)	386	806	813
Avg. mobility under base (cm^2/v-s)	441	946	1036
Base (p-type)			
Surface concentration (/cm^3)	1.2×10^{19}	1.4×10^{18}	1.7×10^{18}
Sheet resistivity (ohms/sq)	124	750	600
Junction depth (μm)	2.0	1.3	1.5
Avg. mobility (cm^2/v-s)	54	124.5	127
Avg. mobility under emitter (cm^2/v-s)	39.6	164	195
Emitter (n^+-type)			
Surface concentration (/cm^3)	6.5×10^{20}	3.4×10^{20}	3.6×10^{20}
Sheet resistivity (ohms/sq)	7	20	16
Junction depth (μm)	1.5	0.8	1.0
Avg. mobility (cm^2/v-s)	47	74	76
Alpha cut off frequency			
NPN (MHz)	143	542	648
PNP (MHz)	51	161	382
Junction capacitance			
Emitter to base @ -3 V (pF/mil^2)	0.42	0.35	0.27
Base to collector @ -3 V (pF/mil^2)			
Collector to substrate @ -3 V (pF/mil^2)	0.08	0.04	0.02

	Present	A	B
Diffused Resistor Values			
Emitter (ohms/square)	7	20	16
Base (ohms/square)	124	750	600
Collector (ohms/square)	100	750	900
Pinched collector region (ohms/square)	472	2380	5290
Pinched base region (ohms/square)	18K	11K	15K

TABLE 6

Size Factors

	Present	Half Size
Basic tolerance dimension (μm)	4	2
Silicon contacts (μm)	4	2
Metal lines (μm)	10	5
Metal spacing (μm)	4	2
Diffused region spacing (μm)	4	2
Diffused collector depth (μm)	4.8	3.5
Typical dimensions		
NPN transistor ($x10^{-5}$ cm^2)	3.17	0.79
PNP transistor ($x10^{-5}$ cm^2)	2.98	0.75
5K resistor ($x10^{-5}$ cm^2)	1.97	0.49
LSI device density		
Regular array (per cm^2)	32,000	128,000
Irregular array (per cm^2)	10,970	43,800
Maximum number of gates per maximum size chip (1 cm^2)		
Regular array	10,670	42,680
Irregular array	3,650	14,600
Alpha cut-off frequency		
NPN (MHz)	125	500
PNP (MHz)	40	150
Junction capacitance		
Base to emitter (pF/mil^2)	0.42	0.35
Base to collector (pF/mil^2)	0.25	0.14
Collector to substrate (pF/mil^2)	0.08	0.04
Normalized area	1	0.25
Power (Normalized for given speed)	1	0.20

SECTION V

TRIPLE DIFFUSED EFL CIRCUITS

In the previous sections the characteristics and fabrication of triple diffused emitter follower logic were considered. The properties of this technology coupled with high yields and inherent process simplicity tend to promote 3D-EFL as an LSI circuit technology. The purpose of this section is to observe some representative 3D-EFL LSI circuit realizations in order to better ascertain the value of the technology for LSI and VLSI implementation. Again the authors are indebted to TRW, from whom this material orginates.

A. Signal Processing Arithmetic Unit

As the name implies, this LSI circuit is an arithmetic unit encompassing such operations as

1. 12 x 12 bit multiplication
2. 12-bit post-operative scaling
3. Product truncation at 12 significant bits
4. Two's complement addition
5. Operand holding with synchronous reset
6. On-chip accumulation.

The arithmetic unit has been designed to be TTL compatible and has tristate outputs. Subsequent design will increase word length from 12 to 16 bits. The unit requires off-chip control and storage.

Table 7 lists important structure and operating characteristics for the arithmetic unit. The arithmetic unit is packaged in a 64 lead flat pack supplied by Koto Ceramic Co., Ltd. (part number KD-74043-A). The package has a 400 mil square geometry die cavity.

B. Configurable Gate Array

The configurable gate array is designed to provide design flexibility based on customer needs. Gate interconnections and connections from gates to pads are specified by the customer. By altering the metallization mask the required gate configurations are realized. The array consists of combinatorial logic gates, including 120 4-input gates, 60 2-input gates, 60 inverters and 60 input-output leads. Gate connections can be specified to form any non-complemented Boolean function of four or less variables. One hundred two

TABLE 7

Arithmetic Unit Characteristics

Basic cell size	392x420 μm (15.68x16.8 mils)
Cell area	164,640 square μm (263.4 square mils)
Approximate device density	4.2 square mils/device
Estimated chip yield	24.6% @ D_o = 2.5/cm^2 (Reference 15)
Number of chips per wafer	19.7
Wafer yield	4.9 chips/wafer
Chip dimensions	315x351 mils = 1.1057x10^5 mils^2
Chip cost	$46.18 at $225/wafer
Total power dissipation	5.14 W
Total current demand	1.028 A
Number of devices	13,796
Dissipation per device	0.37 mW/device, average
Clock period	120 ns
Instruction process time	207 ns (typical), 278 ns (maximum)
Total time allocated	360 ns
Substrate	
Resistivity	1.0 ± 0.2 ohm-cm
Collector	
Junction depth	4.3 ± 0.1 μm
Sheet resistance	150 ± 10 ohm/square
Base	
Junction depth	2.2 ± 0.1 μm
Sheet resistance	138 ± 12 ohms/square
Resistors	
Pinched collector	1000 ± 100 ohms/square
Pinched base	25K ± 2K ohms/square
Alpha cut off frequency	
f_α (NPN)	250 ± 30 MHz
f_α (PNP)	80 ± 15 MHz

configurations are possible. Figure 16 (courtesy of TRW, Redondo Beach, California) is a photomicrograph of the gate array. Table 8 is an overview of characteristics related to the gate array.

Three packages are currently available. These are

1. 40 lead ceramic DIP, 0.6" wide
2. 64 lead ceramic DIP, 0.9" wide
3. 64 lead ceramic square flat pack, 0.9".

At this time, process design specifications are unavailable.

This array is somewhat of a departure from conventional custom LSI design in that it is a "standardized" circuit on a chip which is later modified by alterations to the metallization interconnect mask. The gate array is the only 3D-EFL LSI circuit which embodies design-function standardization.

C. Monolithic 16 x 16 Bit Parallel Multiplier

The monolithic parallel multiplier has been designed to implement rapid processing in avionics applications. The unit uses two's complement arithmetic and features tristate output buffers and time-sharing capabilities. An off-chip control unit is required. Table 9 contains available characteristics of the multiplier and Fig. 17 (courtesy of TRW, Redondo Beach, California) is a photomicrograph of the circuit.

D. Digital Delay Time

The digital delay line is designed to be used in signal processing applications where address control of an FFT processor is required. It contains a group of D flip-flops with input and output signal multiplexers. The outputs are tristate design. Table 10 contains available information pertaining to the digital delay time. The circuit is to be packaged in a 40 lead ceramic dual-in-line package.

E. Remarks

More than 50 LSI designs using 3D-EFL have been produced within the last two years. These circuits extend throughout the ranges of packing density, size, and chip complexity. Four representative circuits have been described in this section; other 3D-EFL realizations include code generators, random logic, arithmetic control units, and a 64-bit correlator. All of these circuits have been fabricated by triple diffusion techniques. Because much

of this work is done for classified projects information concerning the implementation of future designs is not available.

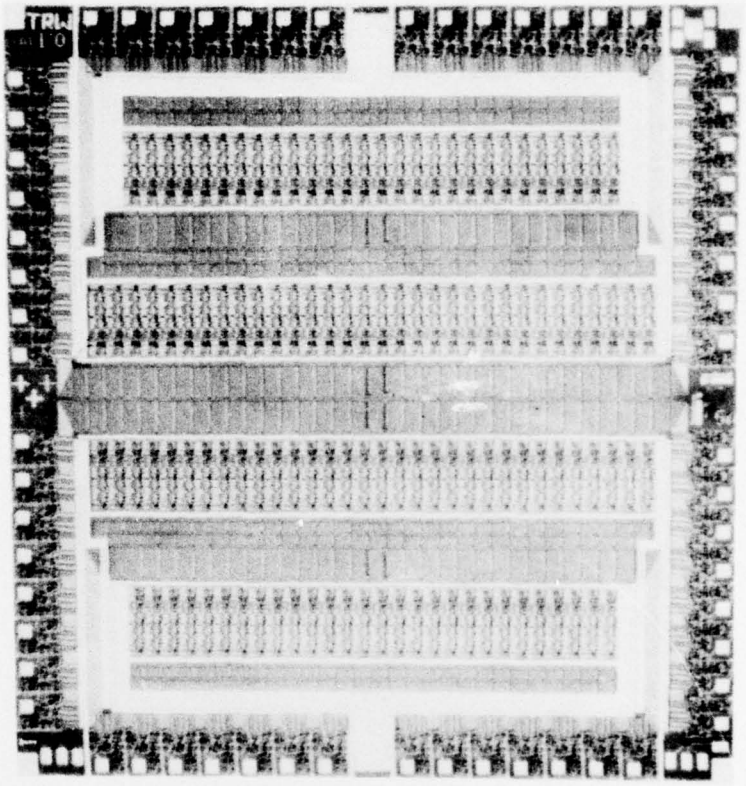


FIG. 16 CONFIGURABLE GATE ARRAY (PHOTO COURTESY OF TRW)

TABLE 8

Configurable Gate Array

Typical inverter

V_{CC} = 5.0 ± 0.5 V	
I_{CC}, average supply current @ 25°C	3.1 mA
V_{IL} = 0.8 V	
V_{IH} = 2.0 V	
V_{OL} = 0.4 V	
V_{OH} = 2.4 V	

NPN output transistors

Sink	10 mA maximum
Source	5 mA maximum

Typical resistor tracking tolerance	5%

Signal propagation time

Inverting gate	12 ns
Non-inverting gate	7 ns

TABLE 9

16 x 16 Bit Multiplier Characteristics

Substrate (p-type) Resistivity	3 ohm-cm
Device count	16,700
Chip size	301 x 279 mils
Device density	5 square mils/device
Approximate number of chips per wafer	19 dice
Yield	3 dice out of 19
Full instruction cycle time	330 ns (maximum)
Multiply time	100 ns
Number of devices within a basic cell	63 devices
Power requirement	5 Watts
Approximate packaged silicon cost	$100

TABLE 10

Digital Delay Line Characteristics

Chip size	177 x 184 mils
Device count	2322 devices
Device density	6.8 square mils/device
Shift register clock frequency	10 MHz (typical)
V_{CC}	5.0 V
Power, average	0.75 W
I_{CC}, average	150 mA

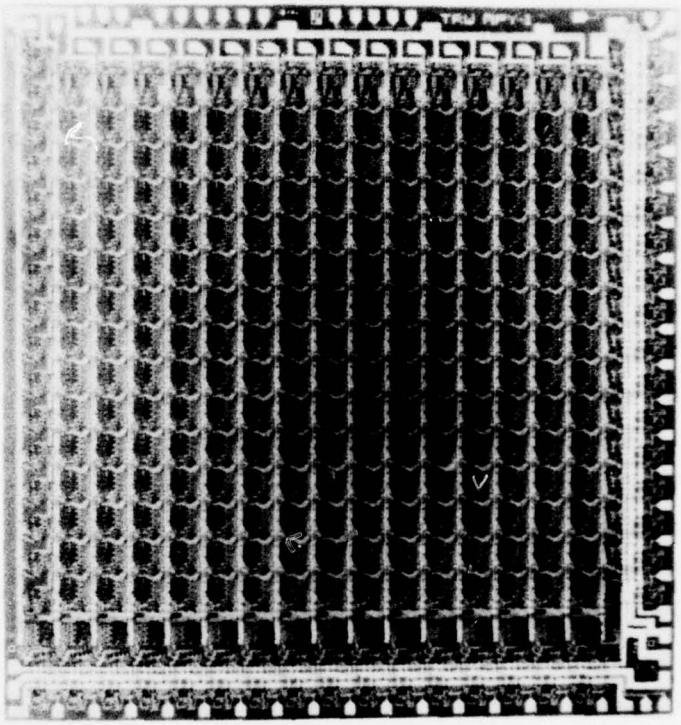


FIG. 17 16 X 16 BIT PARALLEL MULTIPLIER (PHOTO COURTESY OF TRW)

SECTION VI

DISCUSSION AND CONCLUSIONS

In this report the history, development, and performance of 3D EFL LSI circuits has been presented. The advantages and disadvantages will now be discussed and an overall assessment made.

A. Disadvantages of 3D EFL

The apparent disadvantages of emitter follower logic fabricated by a triple diffused process as they have been stated in earlier parts of this report can be summarized as follows.

1. EFL requires signal level restoration.
2. Inverters and complementary transistors are required for full logic capabilities.
3. Vertical PNP transistors have low gain and poor frequency response.
4. The emitter follower is prone to parasitic oscillation.
5. The parasitic collector resistance is high.
6. Power dissipation is high.

The answers to some of these drawbacks are repeated here for convenience. EFL does not require signal restoration if inverters and complementary transistors are used. The need for these is not a real disadvantage since it can lead to more flexible logic, common collector regions, self-isolated components, and hence a high packing density. It is true that gain and frequency response of PNP transistors is low. The disparity between the performance of NPN and PNP transistors appears in all variations of 3D technology, including GIMIC-O and TRW's advanced 3D technology. Of course, high current gains are not a necessity in EFL circuits. It appears that the frequency response can be improved, but will always be limited by the PNP transistor. Users of EFL SSI circuits were cautioned against the possibility of parasitic oscillations. This does not appear to be a problem in LSI circuits.

We have seen that the absence of a buried layer increases the collector bulk resistance. For non-saturating logic the higher $V_{CE(sat)}$ is of no consequence since the circuits are operated in the active region. The parasitic resistance is deleterious however since it contributes to higher

power dissipation. The high dissipation is a serious disadvantage for any technology vying for LSI applications. For the specific circuits mentioned in the last section, all but one have a dissipation greater than 3 watts. No standard package can transfer this much power to the ambient without special heat sinks. The high dissipation of present 3D EFL must therefore be regarded as a severe drawback.

B. Advantages of 3D EFL

The primary advantages of 3D EFL are as follows:

1. Simple processing
2. High speed
3. High yields
4. Radiation hardened
5. High packing density.

To say that an integrated circuit family is simple to fabricate implies that the wafer manufacturing costs are low. The direct costs include materials (substrates, chemicals, glassware, photomasks, etc.), labor, capital equipment, and overhead (utilities, building depreciation or rental, etc.). Each of these depends on the number of processing steps and their complexity. For example, fewer masking levels reduces the costs of manufacturing, cleaning, and inspecting masks; it also implies less chemicals and glassware, less capital equipment, lower labor costs, and less floor space. Ion implantation versus a standard diffusion step requires more capital equipment expenditures but less labor costs and perhaps less breakage and better yields.

A list of the major processing requirements for 3D EFL, standard TTL, and metal gate PMOS is given below. The number of masking levels does not include scratch protection because this is a non-critical step.

3D EFL	Standard TTL	PMOS
5 masks	6 masks	4 masks
2 ion implants	4 diffusions	1 diffusion
1 diffusion	1 epi layer	2 oxidations
4 oxidations	2 oxidations	1 metallization
1 metallization	1 metallization	1 glassivation
1 glassivation	1 glassivation	40 process steps
65 process steps	60-100 process steps	

On this basis, it would seem that wafer fabrication costs would lie somewhere between those of PMOS and TTL for large production quantities. Therefore one could rightfully say that 3D EFL is "simpler" to process than standard TTL, but not as simple as PMOS. It is interesting to note that GIMIC-O is said to have a lower manufacturing cost than PMOS (7). In terms of final parts cost, the wafer probe yield and packing density also have a profound effect.

The speed of several technologies is listed below. The performance of present 3D EFL places it close to standard TTL, significantly better than PMOS (and CMOS) and of course much slower than ECL (and Schottky TTL). SOS MSI circuits are available with clock frequencies to 50 MHz. The conclusion is that 3D EFL is more of a medium-speed technology in its present form.

	3D EFL	Standard TTL	PMOS	ECL
Gate Delay	7-14 ns	10	40	1
Clock Frequency	10-20 MHz	30	2	500

TRW has been able to achieve outstanding yields, characterized by a defect density of 3 defects/cm^2 in the Dingwall model. This is almost an order of magnitude less than typical defect densities for other bipolar integrated circuit technologies. A reasonable figure for PMOS LSI is 3-10 defects/cm^2. Both Motorola and Western Electric with their versions of 3D technology have been able to achieve 6-8 defects/cm^2.

If we assume that new photomasks have a defect density of 1 defect/cm^2 (15), then the use of 5 new photomasks in sequence would yield a total defect density in the Dingwall model of 6 defects/cm^2. It appears then that the high yield of TRW's circuits is due in part to the inherent advantages of the 3D process and in part to the use of high quality masks.

In its tolerance to various forms of radiation, 3D EFL is typical of other bipolar circuits. Its good characteristics in this regard can be attributed to the high surface impurity concentrations and to the attributes of emitter followers.

In evaluating component densities the only fair comparison is among existing integrated circuits, rather then on a proposed circuit or a simplified gate layout basis. The actual component densities of several circuits are tabulated here. These figures are the actual or estimated

component count divided by chip area.

Signetics Utilogic II (SSI)	15,000 components/in^2
Fairchild CμL (SSI)	18,000
3D EFL	100-200,000
LSTTL logic chip	71,000
SOS timing chip	250,000
PMOS microprocessor	130,000
NMOS microprocessor	160,000
CMOS microprocessor	50,000
I^2L microprocessor	52,000
SOS microprocessor	170,000
NMOS dynamic RAM	300-800,000
Isoplanar I^2L RAM	660,000
SOS RAM	370,000

This tabulation shows that 3D EFL component density is comparable to that for MOS and SOS random logic, and much higher than that of CMOS, LSTTL and I^2L random logic. Memories (1K and 4K) are extremely efficient in silicon utilization in all technologies. Of course, these figures are for specific circuits and could vary considerably, especially for newer implementations such as I^2L. Nevertheless one can conclude that 3D EFL is as good as, or somewhat superior to, other forms of random logic circuits.

C. Conclusions

From the customer's point of view, the only attributes of a integrated circuit which need to be considered are price, performance, and availability.

1. Price - The combination of low wafer fabrication cost, high yield, and high packing density would make parts costs lower than bipolar and comparable to PMOS.
2. Performance - By most performance criteria (speed, noise immunity, radiation hardness, reliability) 3D EFL compares reasonably well with other bipolar logic families. The high power dissipation is a severe drawback for LSI circuits.
3. Availability - TRW has recently announced a 16 bit bipolar multiplier which will be available commercially

near the end of 1976. At the present time no other circuits are available. This fact, plus the lack of any second source rules out any serious consideration of EFL for systems which require replacement parts over a long period of time.

D. Recommendation

Because of its general lack of availability, 3D EFL is not recommended for any electronic system which will require replacement parts over an extended period of time.

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